Notes On Pulse Signaling

Jo Ebergen, Steve Furber, Arash Saifhashemi, Naela Nissar, Alex Chow

VLSI Research Group
Sun Microsystems Laboratories
Introduction

- Most common signaling techniques
  - Level signaling
  - Transition signaling
  - Single-track signaling

- Let’s look at pulse signaling
  - Do simple implementations exist?
  - How robust are these circuits?
  - How efficient are these circuits in terms of delay, energy, and area?
Signaling Protocols

- **Level signaling**

- **Transition signaling**
More Signaling Protocols

• Single-track signaling

• Pulse signaling
An Example of a Pulse Module

- The Pulse Repeater
Variations

- Larger pulse width
- Guard against too long input pulse
- Negative pulse implementation
Pulse Merge

- The ‘OR’ for events
Pulse Join

- The ‘AND’ for events

- An incorrect implementation
A Better Pulse Join?

- Negative-pulse implementation

![Diagram of pulse join implementation]
2-by-1 Pulse Join

- Also known as 2-by-1 Decision-Wait
- \((a_0 \text{ AND } c \text{ produces } b_0) \text{ OR } (a_1 \text{ AND } c \text{ produces } b_1)\)
A Better Implementation

- Is negative pulse implementation even better?
Properties of Pulse Modules

- Self-reset produces fixed-width pulse
- Pulse module restores ‘poor’ pulses (Nyström)
- Output always strongly driven
- Condition: Cycle time > 2x Pulse Width
A Comparison

• Compare level signaling with pulse signaling
• Application: a pipeline
• Estimate energy (area) as a function of cycle time
• Analysis based on Logical Effort
• 180nm CMOS TSMC technology
Pipeline with Level Signaling

- Four-phase, level signaling (as in CHAIN)
- Cycle Time: 2x5 = 10 'gate delays'
Pipeline with Pulse Signaling

- Positive or negative pulse implementation
- Cycle time: 6 ‘gate delays’

(req) (1-out-of-4) ack
Energy vs Cycle Time

\[ \tau = 14.5 \text{ps}, \ \varepsilon = 2.8 \text{fJ} \]
Robustness Issues

- Long wires deteriorate pulses
  > What wire length deteriorates pulses beyond detection?

- Capacitive coupling deteriorates pulses
  > Can we quantify effect of coupling on pulses?
Max Wire Length vs Pulse Width

Maximum Wire Length vs. Pulse Width

- Stepup = 3
- Stepup = 4
- Stepup = 5
- Stepup = 6
Effect of Capacitive Coupling

Diagram showing the effect of capacitive coupling on pulse width and normalized timing offset between aggressor and pulse.
Summary

- Pulse signaling is an attractive signaling protocol
- Simple implementation templates exist
- Pulse signaling compares favorably with level signaling wrt energy-vs-delay performance
- Pulse signaling offers good robustness
  > Deals gracefully with long wires
  > Deals gracefully with capacitive coupling
- Negative pulse implementations are better than positive pulse implementations
Concluding Remarks

- More research needed
- Influence of other noise sources?
- Effect of device variations?
- Effect of threshold voltage variations?
- Need to build and test chips
Thank you!

Jo Ebergen
jo.ebergen@sun.com