Process Integration of Photonic Interposer for Chiplet-based 3D Systems

Damien Saint-Patrice
CEA-Leti, Univ Grenoble Alpes
Grenoble, France
damien.saint-patrice@cea.fr

Stéphane Malhouitre
CEA-Leti, Univ Grenoble Alpes
Grenoble, France
stephane.malhouitre@cea.fr

Myriam Assous
CEA-Leti, Univ Grenoble Alpes
Grenoble, France
myriam.assous@cea.fr

Thierry Pellerin
CEA-Leti, Univ Grenoble Alpes
Grenoble, France
thierry.pellerin@cea.fr

Rémi Vélard
CEA-Leti, Univ Grenoble Alpes
Grenoble, France
remi.velard@cea.fr

Leopold Virot
CEA-Leti, Univ Grenoble Alpes
Grenoble, France
leopold.virot@cea.fr

Edouard Deschaseaux
CEA-Leti, Univ Grenoble Alpes
Grenoble, France
edouard.deschaseaux@cea.fr

Maria-Luisa Calvo-Muñoz
CEA-Leti, Univ Grenoble Alpes
Grenoble, France
Maria-luisa.calvomunoz@cea.fr

Karim Hassan
CEA-Leti, Univ Grenoble Alpes
Grenoble, France
karim.hassan@cea.fr

Stéphane Bernabé
CEA-Leti, Univ Grenoble Alpes
Grenoble, France
stephane.bernabe@cea.fr

Yvain Thonnart
CEA-Leti, Univ Grenoble Alpes
Grenoble, France
yvain.thonnart@cea.fr

Jean Charbonnier
CEA-Leti, Univ Grenoble Alpes
Grenoble, France
jean.charbonnier@cea.fr

***Abstract*— To overpass the bandwidth and the latency limitations of electrical links, the next breakthrough in high performance computing integration will eventually come through photonic technology and Optical Network-on-Chip (ONoC). This work introduces a global architecture of an ONoC and reports the detail integration and fabrication on the 200 mm Leti's platform of a Si photonic interposer on SOI wafers. Active photonic circuit operating at 1310 nm wavelength, 12 µm diameter 100 µm height Through Silicon Via (TSV) middle process, four metal layers Back-End Of Line (BEOL) with µ-pillars and backside redistribution layer with thermal cavity above heaters have been successfully achieved. Morphological characterizations as cross-sections assess the process developments and integration results. Optical propagation losses measured on Rib and Deep Rib structures and insertion losses on Single Polarization Grating Couplers (SPGC) structures both at the end of the active photonic and after TSV / BEOL processes show no deviation. The TSV middle resistance is evaluated below 22 mΩ with a yield greater than 95 %. Finally, all individual process blocks required for the functional ONoC system, especially Ring Modulators is discussed regarding their successful optimized co-integration.**

Keywords—Photonics, Interposer, silicon ring modulator, TSV Mid, Optical Network on Chip, High Performance Computing, Chiplet.

I. Introduction

In the context of High Performance Computing (HPC) and Big Data application, modular and scalable architectures are emerging involving chiplets approach compare to large and costly monolithic chips [1]. The system architecture and performance then rely on the number and type of chiplets but also on their interconnections scheme, pitch and latency. Starting from advanced Ball Grid Array (BGA) approach, to passive interposer and finally active interposer [2], network on chip architectures have proven their interest thanks to high density integration, high bandwidth in between chips, reduce latency, IP reuse and cost efficiency. Following this trend, an opportunity has been identified with the recent maturity of silicon photonic devices leading to the introduction of Optical Network on Chip (ONoC) paradigm. Recently, industries are rising great expectations based on this approach. Silicon photonic (SiPho) interposer could offer a step further in latency reduction, bandwidth increase and decrease of power consumption [3] by using photonic waveguides interconnects instead of electrical links.

This study will focus on the SiPho interposer process integration and technology development. Previous studies have reported on SiPho interposer, Through Silicon Via (TSV) and wave-guide or Micro Ring Resonator (MRR) co-integration [4-9] however, none of them has described a full operating system. The following paper will first briefly introduce the POPSTAR system components and architecture followed by the design and technological stack of the corresponding SiPho interposer [3]. The detail of the fabrication process, including photonic Front End Of Line (FEOL), TSV middle process, Back End of Line (BEOL) and backside process will then be presented and discussed to end with optical and electrical test results.

II. Design of Silicon Interposer

The targeted ONoC system corresponding to POPSTAR architecture is based on micro ring photonic link as described in [3]. 4 chiplets and 6 Electro-Optical (E/O) conversion chips are face to face stacked on a SiPho interposer as represented on Fig. 1. This assembly is finally mounted on a BGA.

2377-5726/23/$31.00 ©2023 IEEE
DOI 10.1109/ECTC51909.2023.00009

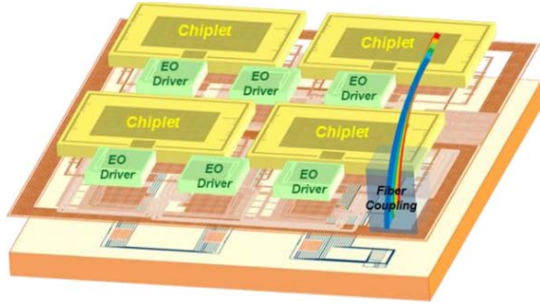
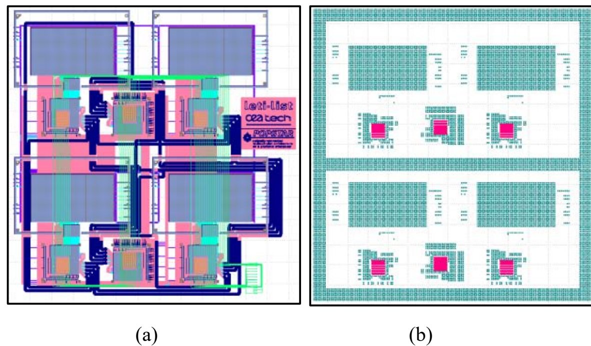


Figure 1. Schematic view of the ONoC system

The 4 chiplets embed 16 computation cores each. E/O interface drivers are in charge of buffering, routing, arbitration, serialization, driving and thermal tuning of MRR modulators and filters. They are designed to be standard and replicable. The photonic interposer host the 10 dies on its top surface thanks to microbumps/micropillars matrices. As described in the layout of Fig. 2, the interconnections between the chiplets and the E/O dies are achieved thanks to the 4 layers of BEOL of the SiPho interposer. Waveguides and active photonic devices such as photodiodes and MRR allow wavelength division multiplexing photonic links between E/O dies responsible for the high-density bandwidth, low latency and low power consumption [3]. In addition to this, each MRR is thermally isolated with a backside cavity in order to reduce the thermal tuning power needed [10]. Power signals come from the backside of the interposer through TSV connected to backside Redistribution Layer (RDL) and BGA.



(a) (b)

Figure 2. Layout (GDS extract) of SiPho interposer a) Front side layers (green: waveguide, light blue: microbumps, pink and dark blue: BEOL) and b) Back side layers (cyan: balls, red: backside cavities)

A technological cross-section of the interposer is presented in Fig. 3, introducing micropillars, BEOL layers, active photonics, backside cavities, TSV, RDL and solder balls.

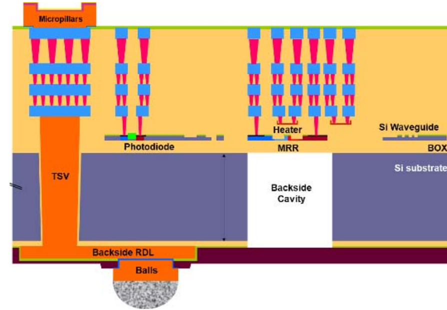


Figure 3. Schematic technological cross section of the SiPho interposer

III. FABRICATION PROCESSES

In this section, POPSTAR SiPho interposer process flow is presented from the front-end photonic to the backside processes. Different technological building blocks can be defined as represented on the following figure.

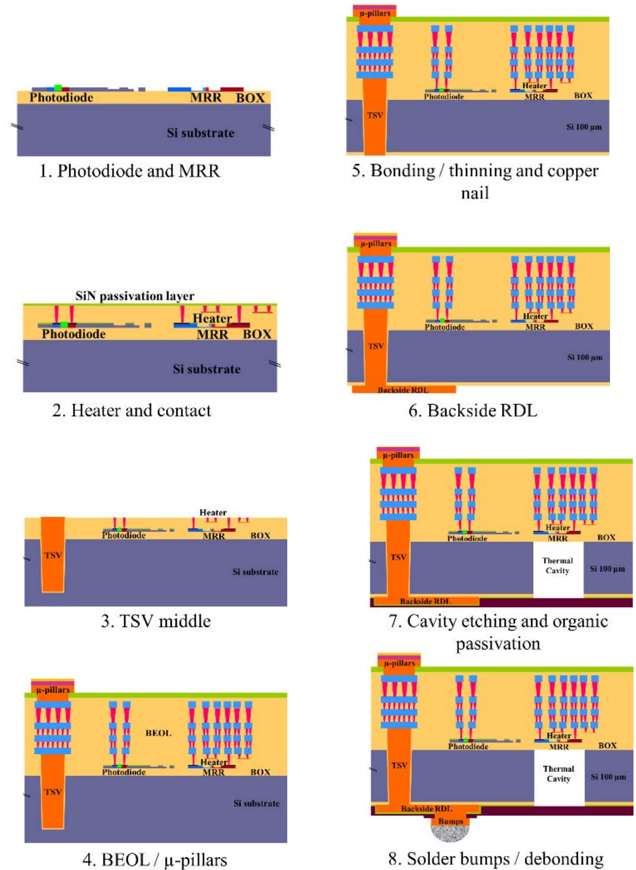


Figure 4. POPSTAR SiPho interposer schematic process flow

A. Front-end photonic

Photonic silicon components were fabricated on 200 mm silicon fabrication platform at CEA-LETI on Silicon-On-Insulator (SOI) substrates featuring a 310 nm thick silicon film on top of an 800 nm thick Buried Oxide (BOX) [11].

Fabrication started with various implantation steps to define PN and PIN junctions of MRR, and electrical access paths to MRR and photodiodes. Photonic silicon structures were then patterned using Si_3N_4 hard mask. 3 levels of DUV photolithography (193 nm and 248 nm) were used to define 3 silicon thicknesses to obtain waveguides routing and Single Polarization Grating Coupler (SPGC), featuring 300 nm thick waveguides and 165 nm thick Rib-slab, and MRR structure with 300 nm thick ring waveguides and 65 nm thick Deep-Rib slab. The different silicon thicknesses of the silicon photonic devices are presented in Fig. 5.

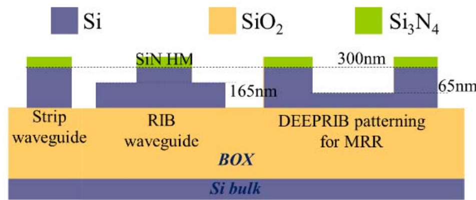


Figure 5. Schematic cross-section of strip waveguide, Rib-waveguide and Deep-rib level in MRR

Following Si patterning, additional implantation levels were performed on the slab of the MRR to enhance modulation performances.

After High Density Plasma Chemical Vapor Deposition (HDP-CVD) SiO_2 encapsulation of silicon structures and planarization, butt-coupled SiGeSi photodiodes were fabricated by patterning a cavity in silicon using the SiO_2/Si_3N_4 dielectric stack as hard mask [12]. After partial etching of the cavity in silicon and surface preparation, Germanium is grown on Silicon thanks to selective epitaxy using a two-steps Reduced Pressure Chemical Vapor Deposition (RPCVD) process. Excess of Germanium was removed by CMP stopping on SiO_2 top surface. A SiO_2 layer was then deposited to cap the Ge photodiode. Fig. 6-a represents a schematic cross section of the resulting Ge photodiode, and Fig. 6-b shows the FIB cross-section image of Ge photodiode after SiO_2 capping.

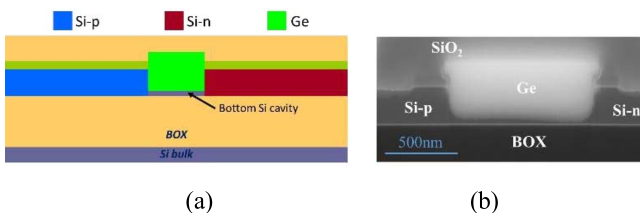


Figure 6. Ge photodiode (a) schematic cross-section and (b) cross-section FIB image

To enhance electrical contact on active photonic devices, silicidation was performed at the surface of the highly doped silicon areas defined as electrical access paths to MRR and photodiodes. Dielectric stack was etched down to doped silicon, and a $TiSi_2$ silicide was formed by deposition of a thin Ti/TiN stack on Si followed by a thermal anneal. After wet removal of unreacted Ti/TiN, a second thermal anneal was done to stabilize the 20 nm silicide layer. A thick SiO_2 layer was then deposited and planarized at a thickness of 600 nm thick over the 300 nm thick silicon photonic structures.

MRR resonant frequency is controlled by using thermal heater on top of MRR waveguide, as shown on MRR design in Fig. 7-a, and schematic cross-section in Fig. 7-b.

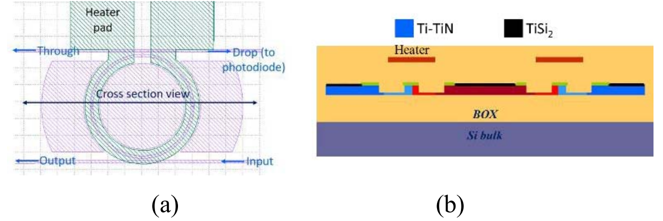


Figure 7. (a) Top view of MRR with heater and (b) schematic cross-section of MRR with heater

Thermal heaters were fabricated by deposition of a Ti 10 nm / TiN 100 nm stack which was patterned by dry etching. A microscope picture of a heater on top of a MRR is shown in Fig. 8. Heaters were encapsulated by a 300 nm thick planarized SiO_2 layer.

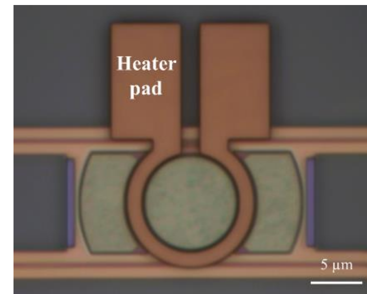


Figure 8. Optical microscope picture of Ti/TiN heater on top of MRR

Metal contacts started first with dry etching of the heater contacts in 300 nm thick SiO_2 layer on top of the heater. Then both MRR and photodiodes contacts were processed by etching the dielectric stack down to the $TiSi_2$ silicide layer on top of Si photonic devices. One step W deposition was done to fill both heater, photodiode and MRR contacts. Excess of W was removed by CMP. A cross-sectional view of the Ge photodiode with W contacts is shown in Fig. 9.

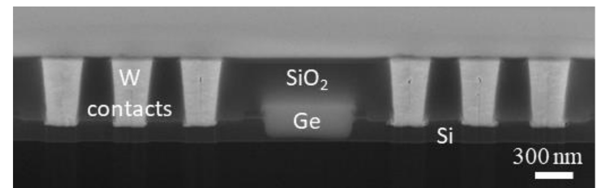


Figure 9. Germanium photodiode with W contacts

60 nm PECVD SiN passivation layer was deposited before TSV process. A schematic cross section of the full Photonic Integrated Circuit (PIC) after contact definition and passivation is presented in Fig. 10.

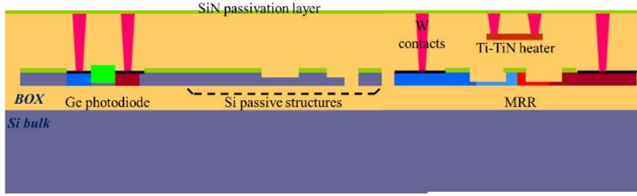


Figure 10. Schematic cross-section of the full PIC before TSV processing

B. *TSV middle*

The TSV process selected for POPSTAR interposer was a TSV middle like with a 12 µm diameter and 100 µm thick. The TSV etching was performed in two steps. Firstly, the dielectric photonic stack (SiN/SiO_2) was etched with Reactive Ion Etching (RIE) process. Secondly, the silicon was etched with Deep Reactive Ion Etching (DRIE) with Bosch process through patterned photoresist (Fig. 11).

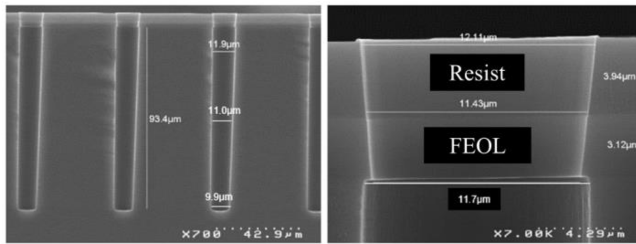


Figure 11. SEM cross-section of TSV middle profile after DRIE

The TSV isolation was achieved with 300 nm of Sub-Atmospheric Chemical Vapor Deposition (SACVD) and 100 nm of Plasma Enhanced CVD (PECVD) silicon oxide. Then barrier and seed layers were deposited. The deposition sequence consisted in a Ti PVD adherence layer, a TiN CVD barrier and a Cu PVD seed layer. As the conformality of the Cu PVD process is limited an additional electro-grafted Cu layer is plated to ensure proper seed continuity across the TSV (Fig. 12-a).

TSV filling was performed with electro chemical deposition (ECD) of Cu with an optimized bottom-up filling recipe. This allowed filling the TSV with a remaining Cu surface thickness lower than 3 µm (Fig.12-b).

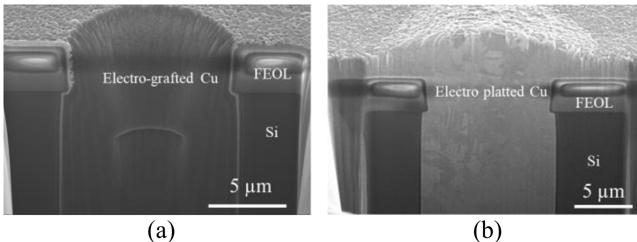


Figure 12. FIB/SEM cross-section of TSV middle (a) with Cu electro-grafted and (b) with Cu electro plated

TSV was then annealed at 400°C with a specific thermal profile to minimize the stress of the Cu (Fig. 13).

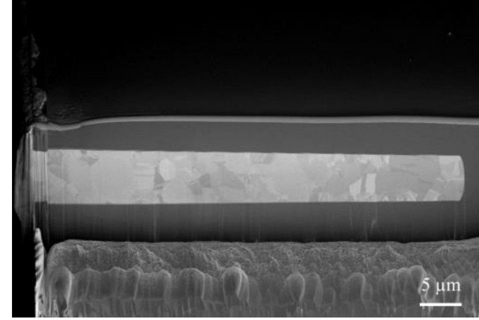


Figure 13. FIB/SEM cross-section of TSV middle after annealing

The last processes were the 2 steps of Chemical Mechanical Polishing (CMP). The first step was dedicated to Cu and barrier layers with selective etch stop on TSV isolation silicon oxide layer. The second step was dedicated to dielectric SiO_2/SiN layers with etch stop on the 300 nm diameter W contacts. This step was challenging mainly due to the TSV Cu opening during the CMP process (Fig. 14).

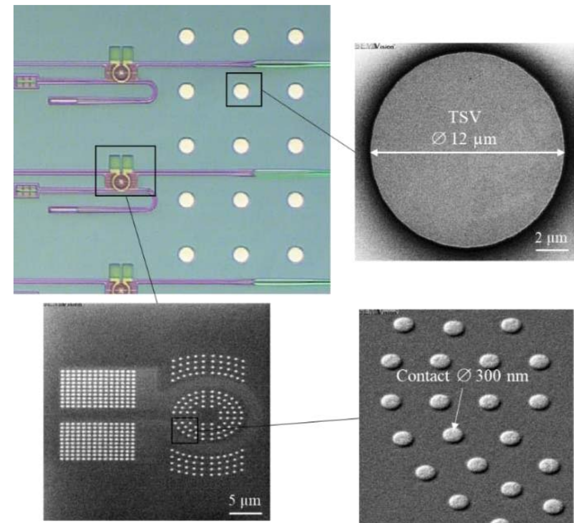
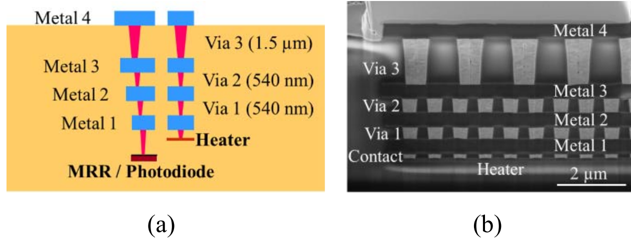


Figure 14. Optical and SEM top views of FEOL photonic with TSV embeded

C. *BEOL*

The BEOL stack is composed of 4 levels of metal routing. As shown in Fig. 15-a, the 3 first levels are identical and are made of a 540 nm Ti-TiN / AlCu / Ti-TiN multilayer metal stack deposited by PVD separated by PECVD SiO_2 interlayer. Each dielectric layer was planarized with CMP process. 300 nm width square contacts were patterned by RIE in the SiO_2 inter-metal layer, filled with W and planarized.

The fourth metal level is identical in thickness than the 3 first metal levels but the interlayer thickness of Via 3 was increased to 1.5 µm for RF functionality purposes. In consequence, the contact dimension was also increased to 750 nm width square contact. Cross-section FIB-SEM image of the full BEOL is presented in Fig. 15-b.



(a) (b)

Figure 15. Full BEOL with 4 levels of metal (a) schematic cross-section and (b) cross-section FIB-SEM image

Final passivation was performed with a planarized 500 nm of SiO_2 PECVD and 600 nm of SiN PECVD. The pad opening was done with a positive resist and the dielectric stack was etched by RIE process.

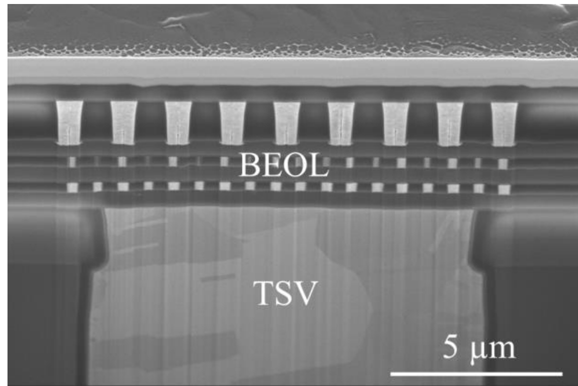


Figure 16. FIB-SEM cross-section of TSV middle with the 4 levels metal of BEOL

D. µ-pillars

The last frontside technological block was the µ-pillars processes. First, Ti/Cu seed layer of 100 nm and 400 nm respectively was deposited by PVD. Lithography was achieved with 12 µm thick positive resist, with a Critical Dimension (CD) of 20 µm and a pitch of 20 µm. µ-pillars were grown by electroplating of 5 µm Cu, 2 µm Ni and 0.3 µm Au. The resist was then stripped and the seed layer removed by wet etching.

E. Backside processes

1) Si thinning and Cu nail revealing

To process wafer's backside, a temporary bonding was performed with 20 µm thick adhesive polymer on 725 µm bulk silicon carrier. Thinning of the interposer wafer was achieved by coarse and fine grinding. Wet silicon stress release finally decreased the thickness to (110 ± 1) µm. Residual silicon thickness above TSV was monitored by infrared interferometry.

Cu nails were revealed with SF_6 RIE process with a thickness range from 3 to 6 µm. A low temperature silicon oxide 2 µm thick was deposited by PECVD. Finally, CMP process was done to remove the dielectric and to open the Cu of the TSV (Fig. 17).

2) Backside RDL, cavity etching and passivation

A seed layer composed of 100 nm Ti and 200 nm Cu was deposited by PVD process prior to positive resist redistribution layer (RDL) line/space 10/10 µm photolithography. After O_2 plasma treatment, 3 µm thick Cu was platted by ECD and the seed layer was wet etched (Fig.17).

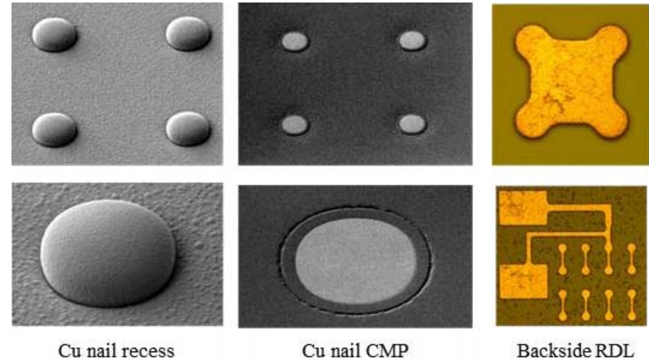
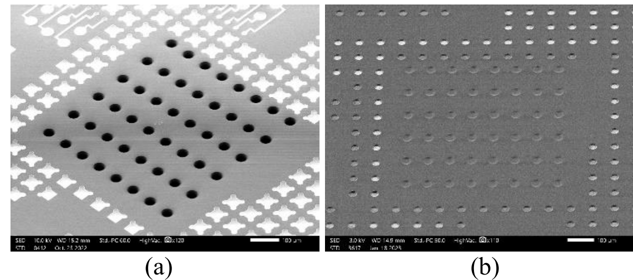


Figure 17. SEM and optical images of the Cu nail and RDL processes

Low temperature SiN layer 100 nm was deposited by PECVD to avoid Cu diffusion in the passivation and to protect it during the plasma steps. Then 40 µm diameter cavities were etched above the ring resonators from the bulk silicon to the BOX. Low Temperature Curing (LTC) passivation polymer 8 µm thick was patterned on RDL with mask aligner lithography and annealed at 230 °C during 3 h under N_2 atmosphere. Dedicated spin coating process was developed to cover the cavities.



(a) (b)

Figure 18. SEM images of RDL and thermal cavities (a) before and (b) after organic passivation

3) Solder bumps and debonding

Firstly, Ti 200 nm / Cu 400 nm seed layers were deposited on the LTC passivation layer. Positive resist was spin on to achieve a thickness of 40 µm. Lithography was done by mask aligner with 40 µm bump diameter and 40 µm space. Bumps were grown by ECD of 5 µm Cu, 2 µm Ni and 17 µm SnAg. The resist was then stripped and the seed layer etched.

The wafers were finally debonded on dicing tape, cleaned to remove adhesive residues and ready for the packaging process.

IV. RESULTS AND DISCUSSION

Electrical tests were performed all along the process to evaluate the photonic structures and the interconnections with dedicated test structures.

A. Photonic passive structures and active devices characterization

All characterization on passive Si structures and photodiodes were performed after TSV processing at metal 1 level. The waveguide propagation losses were extracted using waveguide spirals test structures with various lengths for Rib and Deep-Rib waveguides. An example of measurements for 1.4 cm long waveguide spiral are presented in Fig. 19.

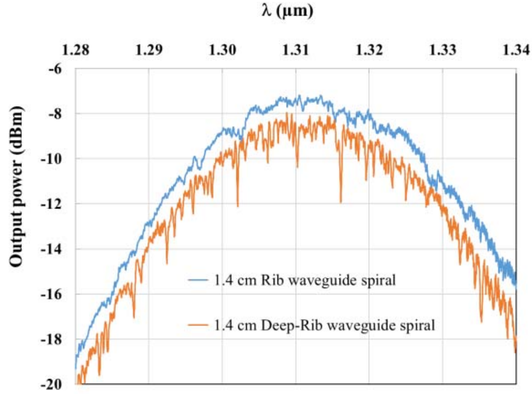


Figure 19. Output power vs wavelength characteristics for Rib and Deep-Rib waveguide spirals

Mean value of SPGC insertion losses and waveguide propagation losses measured on several wafers are summarized in Table 1.

TABLE I. SPGC AND SI WAVEGUIDES MEAUSRED PARAMETERS

SPGC Loss (dB)	SPGC central wavelength (nm)	Rib Waveguide Propagation Loss ($dB.cm^{-1}$)	Deep-Rib Waveguide Propagation Loss ($dB.cm^{-1}$)
3.27 +/- 0,2	1308 +/- 8	0.32 +/- 0,05	0.81 +/- 0,15

The minimum output power is well centered at the nominal 1310 nm wavelength. Typical waveguide propagation loss of 0.3 $dB.cm^{-1}$ is measured on Rib waveguide, mainly used for optical routing. Due to thinner slab, higher propagation loss is measured on Deep-Rib waveguides which are only used in specific devices like MRR [12].

Conventional I-V curves of photocurrent for different illumination powers and dark current of the photodiode (lateral Si/Ge/Si heterojunctions photodiode with 1 µm width for 15 µm long intrinsic Ge area) are shown in Fig. 20.

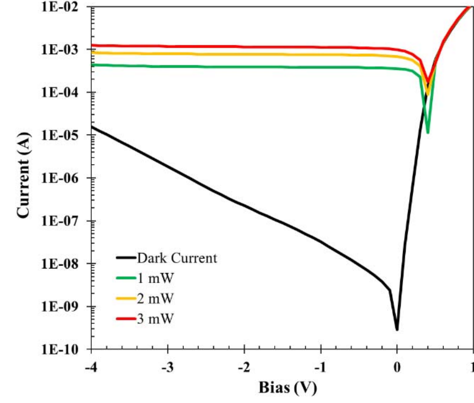


Figure 20. Dark current and photocurrent for various laser power vs voltage bias of 15 µm long photodiode with 1 µm intrinsic Ge width

The photodiode responsivity is extracted from I-V curves and is presented as a function of the reverse bias in Fig. 21.

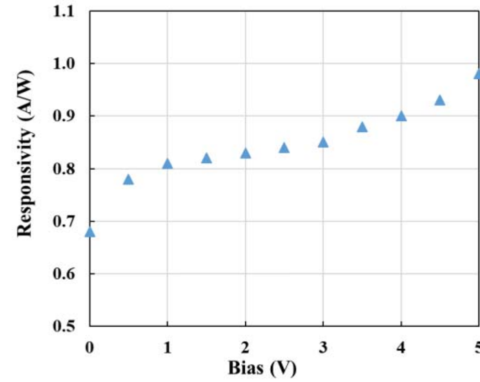


Figure 21. Photodiode responsivity and dark current vs voltage bias

A responsivity higher than 0.8 A/W for 1 V voltage bias shows that the performances of these photodiodes are in accordance with the standard specifications of Ge photodiodes.

The fabricated circuits use two types of MRR:

- PN junction based microring modulator, for data encoding
- PIN junction based microring filter, to switch and route the data

For the PN ring modulators, typical optical response at several reverse DC bias measured on pathfinder lot wafers is shown in 0. The modulation efficiency is calculated to be about 10 pm/V. From the Through measurement (solid lines), the quality factor is estimated to be about ~20 600, which corresponds to an optical 3 dB bandwidth of about 11 GHz. Such bandwidth is sufficient for operation at 10 Gbit/s and beyond. For the data switching/routing, the PIN junction is used in injection regime, leading to very high attenuation (Fig. 23). Thus, under 1 V forward bias, the extinction ratio already reach 18 dB for roughly -3 dB of Drop port insertion losses, and can reach up to 27 dB at 2 V bias, at the price of higher losses.

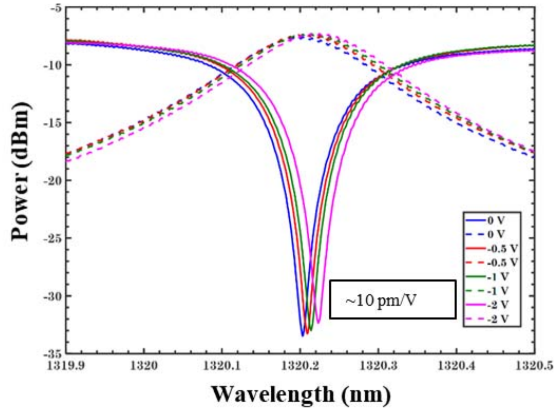


Figure 22. Through (solid lines) and Drop (dashed lines) optical power for the PN microring resonator function of the wavelength and reverse bias

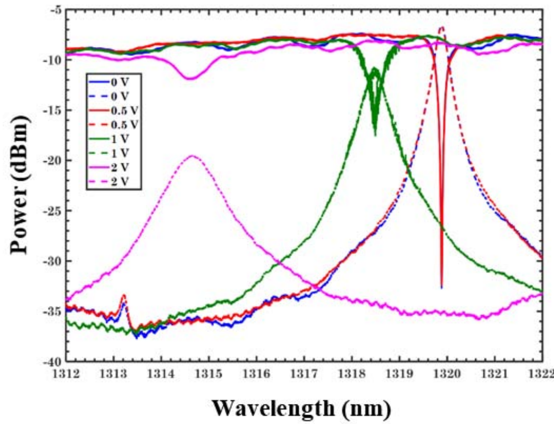


Figure 23. Through (solid lines) and Drop (dashed lines) optical power for the PIN microring resonator function of the wavelength and forward bias

B. DC structures and characterization

In order to check the integrity of the electrical performances of each metal layer of the back-end, sheet resistance and leakage current were measured on 2 µm width, 2 µm space metal comb serpentine pattern 2440 µm length. Fig. 24 shows the final measurements after metal 4 process completion. The sheet resistance of metal 1 to metal 3 is repeatable and evaluated at (74 ± *3)* mΩ/sqr which correspond to an estimated aluminum resistivity of 3.2 Ω.m. Metal 4 are tested after patterning without passivation on top. This difference explains the lower sheet resistivity (69 ± *3)* mΩ/sqr than other metals. Regarding the leakage current, measurements confirm that the technological process steps have almost no impact (Fig. 25).

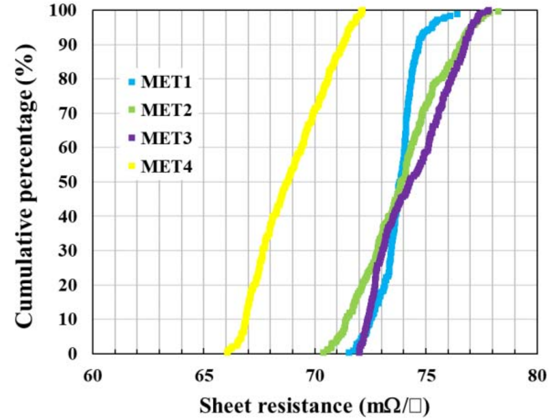


Figure 24. Back-end sheet resistance

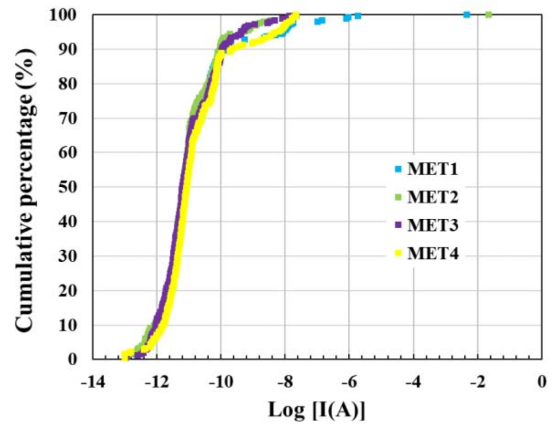


Figure 25. Back-end leakage current

The contact resistance between each back-end layer was evaluated with Kelvin structures. Fig. 26 presents the via resistance between each metal layer. Via 1 and Via 2 are identical (300 nm diameter and 540 nm thick). Via 3 was larger and thicker than the previous one (750 nm diameter and 1500 nm thick) for RF reasons and explain the lower via resistance.

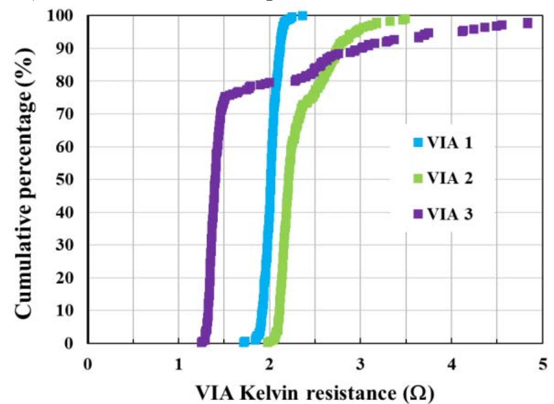


Figure 26. Back-end Via Kelvin resistance

To characterize TSV resistance, standard TSV kelvin structures are measured for 3 types of TSV diameters: 11 µm, 12 µm which is the reference and 13 µm (Fig. 27). As expected TSV resistance decreases with the diameter.

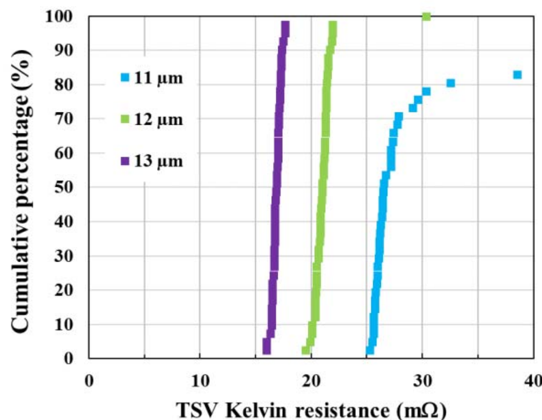


Figure 27. TSV Kelvin resistance with TSV diameter

The Kelvin resistance value of 12 µm diameter TSV is well centered on (21 ± 3) mΩ which is close to the expected theoretical value.

V. CONCLUSION

A full ONoC system for high performance computing and its associated process flow for fabrication have been introduced in this study. Each elementary process module has been described and tested. TSV co-integration with photonic modules has been successfully achieved. For the optical performances, Rib waveguide exhibits a propagation loss as low as 0.32 $dB.cm^{-1}$, PN microring resonator has a modulation efficiency of 10 pm/V and PIN microring resonator has an extinction ratio in the range of 20 dB for 1.5 V bias. For the interconnection performances, each metal routing level shows a repeatable sheet resistance of (74 ± 3) mΩ/sqr with high via yields. Through silicon vias have been measured with mean resistance of (21 ± 3) mΩ with yields higher than 95 % and a low dispersion.
These results will give essential data for the system design and finally pave the way for the Popstar demonstrator currently in fabrication at Leti.

VI. ACKNOWLEDGMENT

The project team would like to thanks P.E Philip, M. Gottardi, G. Romero, T. Magis, S. Dominguez, C. Pellissier, and all our colleagues of Leti silicon process line. Great thanks also to C. Brunet-Manquat, for its contribution to FIB/SEM morphological characterizations and to P. Grosse, K. Ribaud and A. Myko for optical testing.

REFERENCES

[1] D. Dutoit *et al.*, « How 3D integration technologies enable advanced compute node for Exascale-level High Performance Computing?”. 2020 IEEE *International Electron Devices Meeting* (IEDM), Dec 2020 pp.15.3.1-15.3.4, ⟨10.1109/IEDM13553.2020.9372037⟩.

[2] P. Vivet *et al.*, "2.3 A 220GOPS 96-Core Processor with 6 Chiplets 3D-Stacked on an Active Interposer Offering 0.6ns/mm Latency, 3Tb/s/mm2 Inter-Chiplet Interconnects and 156mW/mm2@ 82%-Peak-Efficiency DC-DC Converters," 2020 IEEE *International Solid- State Circuits Conference* - (ISSCC), 2020, pp. 46-48, doi: 10.1109/ISSCC19947.2020.9062927.

[3] Y. Thonnart *et al.*, “POPSTAR: a Robust Modular Optical NoC Architecture for Chiplet-based 3D Integrated Systems,” *Proc. DATE*, 2020, p. 6.

[4] Y. Yang *et al.*, “Through-Si-via (TSV) Keep-Out-Zone (KOZ) in SOI Photonics Interposer: A Study of the Impact of TSV-Induced Stress on Si Ring Resonators,” *IEEE Photonics Journal*, vol. 5, no. 6, pp. 2700611–2700611, Dec. 2013, doi: 10.1109/JPHOT.2013.2285707.

[5] B. Snyder *et al.*, “Packaging and Assembly Challenges for 50G Silicon Photonics Interposers,” in *Optical Fiber Communication Conference*, OSA Technical Digest (online) (Optica Publishing Group, 2018), paper Tu2A.3.

[6] L. Bogaerts et al., "High-Speed TSV Integration in an Active Silicon Photonics Interposer Platform," 2018 IEEE *SOI-3D-Subthreshold Microelectronics Technology Unified Conference* (S3S), 2018, pp. 1-3, doi: 10.1109/S3S.2018.8640164.

[7] D. -W. Kim *et al.,* "3D System-on-Packaging Using Through Silicon Via on SOI for High-Speed Optcal Interconnections with Silicon Photonics Devices for Application of 400 Gbps and Beyond," 2018 IEEE 68th *Electronic Components and Technology Conference* (ECTC), 2018, pp. 834-840, doi: 10.1109/ECTC.2018.00129

[8] B. Sirbu *et al.,* "3D Silicon Photonics Interposer for Tb/s Optical Interconnects in Data Centers with Double-Side Assembled Active Components and Integrated Optical and Electrical Through Silicon Via on SOI," 2019 IEEE 69th *Electronic Components and Technology Conference* (ECTC), 2019, pp. 1052-1059, doi: 10.1109/ECTC.2019.00165

[9] P. Tissier *et al*, “Co-integration of TSV mid process and optical devices for Silicon photonics interposers,” in *Electronics System-Integration Technology Conference (ESTC) 2020 IEEE 8th*, pp. 1-5, 2020

[10] P. Tissier *et al.,* "Backside cavities for thermal tuning optimization of silicon ring resonators," 2021 IEEE 71st *Electronic Components and Technology Conference* (ECTC), 2021, pp. 1667-1672, doi: 10.1109/ECTC32696.2021.00264.

[11] B. Szelag *et al*, “Multiple wavelength silicon photonic 200mm R&D platform for 25Gb/s and above applications”, SPIE Photonics Europe, *2016 - Proceedings of the SPIE, Volume 9891, id. 98911C 15 pp. (2016)*

[12] S. M. Lindecrantz and O. G. Hellesø, "Estimation of Propagation Losses for Narrow Strip and Rib Waveguides," in IEEE Photonics Technology Letters, vol. 26, no. 18, pp. 1836-1839, 15 Sept.15, 2014, doi: 10.1109/LPT.2014.2337055.

[13] Virot, L. *et al.* “Integrated waveguide PIN photodiodes exploiting lateral Si/Ge/Si heterojunction”, *Optics Express* 25, 19487 (2017).