A Study on the Surface Activation of Cu and Oxide for Hybrid Bonding Joint Interface

Bohee Hwang
Advanced Package Business Team
Samsung Electronics Co., Ltd,
Cheonan-si, South Korea
bohee.hwang@samsung.com

Sanwi Kim
Test & System Package
Samsung Electronics Co., Ltd,
Hwaseong-si, South Korea
sanwi.kim@samsung.com

Jeonghwan Lee
Test & System Package
Samsung Electronics Co., Ltd,
Hwaseong-si, South Korea
jeongh15.lee@samsung.com

Soochwon Lee
Advanced Package Business Team
Samsung Electronics Co., Ltd,
Cheonan-si, South Korea
soohwany.lee@samsung.com

Youngkun Jee
Advanced Package Business Team
Samsung Electronics Co., Ltd,
Cheonan-si, South Korea
youngkun.jee@samsung.com

Sangeheon Park
Advanced Package Business Team
Samsung Electronics Co., Ltd,
Cheonan-si, South Korea
sc99.park@samsung.com

Gyeongjae Jo
Advanced Package Business Team
Samsung Electronics Co., Ltd,
Cheonan-si, South Korea
gjae.jo@samsung.com

Kwangbæ Kim
Advanced Package Business Team
Samsung Electronics Co., Ltd,
Cheonan-si, South Korea
kb4021.kim@samsung.com

Sungjin Han
Advanced Package Business Team
Samsung Electronics Co., Ltd,
Cheonan-si, South Korea
sj0429.han@samsung.com

Ilhwan Kim
Advanced Package Business Team
Samsung Electronics Co., Ltd,
Cheonan-si, South Korea
ilhwan77.kim@samsung.com

Jumyong Park
Advanced Package Business Team
Samsung Electronics Co., Ltd,
Cheonan-si, South Korea
jumyong.park@samsung.com

Hyunchul Jung
Advanced Package Business Team
Samsung Electronics Co., Ltd,
Cheonan-si, South Korea
hyun-chul.jung@samsung.com

Sanwi Kim
Test & System Package
Samsung Electronics Co., Ltd,
Hwaseong-si, South Korea
sanwi.kim@samsung.com

Dongwoo Kang
AVP Manufacturing Technology Center
Samsung Electronics Co., Ltd,
Cheonan-si, South Korea
donwoo0305.kang@samsung.com

Un-Byeong Kang
Advanced Package Business Team
Samsung Electronics Co., Ltd,
Cheonan-si, South Korea
ub.kang@samsung.com

Abstract—Hybrid copper bonding technology (HCB) has been developed to reduce the joint gap of stacked chips to the limit for miniaturization of I/O pitch and high heat dissipation. Especially, a critical parameter for multi stack applications is to enhance the bonding strength of oxide interfaces in die-to-wafer (D2W) bonding integration by the surface activation process including plasma treatment, hydration and cleaning before a chip to chip bonding step. Applying the established bonding technology, chemical mechanical polishing (CMP), and the optimized plasma surface activation process, we successfully demonstrated 3D DRAM packages up to 16 stacks. Despite the current development of surface activation sequences, detailed mechanisms of improved bonding strength related to plasma condition have yet been evaluated at the chip level. In this study, we discuss the effect of different plasma treatments on the bonding strength between the oxide interfaces. In particular, a methodology to evaluate oxide interface is proposed. To analyze the quality of the bonding interface of 16 stacked chips in HCB, it is crucial to measure the bonding strength for the bonded thin dies, which have a limitation to evaluate by utilizing conventional die shear test. We have established a novel method of measuring die level bonded interface by applying modified single-beam cantilever (SBC) method with stacked thin dies. By the optimum surface activation and bonding process through the developed analysis method, we have achieved 16 stacked D2W package.

Keywords—Hybrid bonding, D2W, single beam cantilever, bonding strength, plasma treatment

I. INTRODUCTION

Currently, the demand for faster servers with more memory has increased as the amount of data continues to increase. To resolve the data explosion, the advanced package technology has focused on increasing I/O density and faster connections between chips by 3D integration. However, conventional flip-chip bonding using micro bump has a limitation to be applied in fine pitch due to the short risk of micro bump. Moreover, the low thermal conductivity of the gap-fill material leads to high vertical thermal resistance. To resolve these problems, HCB is the attractive approach to achieve submicron interconnect pitches[1-4]. HCB is an advanced die-stacking technology that has enabled the development of heterogeneous integration with tighter interconnection pitches. Hybrid bonding stacks and connects chips using copper-to-copper interconnects; thereby providing higher densities and bandwidths compared with those provided by existing chip stacking interconnect schemes. Especially, the development of the stacking technology utilizing D2W hybrid bonding is
limited by the following issues: 1) handling the warpage of the thin chip, 2) controlling the Cu dishing topology in angstrom level, and 3) optimizing the surface activation treatment before bonding (without suitable condition, it may lead to void in the device causing reliability problem)

To achieve multi chip stacking with more stacked chips without void, the surface activation process of Cu PAD, and surrounding oxide surface before bonding is important for the good bonding quality which affects the electrical performance and the reliability. HCB process includes chemical mechanical planarization (CMP) for the smooth surface of the oxides and the control of Cu dishing, and plasma treatment and deionized (DI) water rinse to form hydrophilic surface with hydroxyl group prior to die to wafer bonding[5,6]. After this process, three interfaces are formed including Cu-Cu, oxide-oxide, and Cu-oxide. Especially, increasing the bonding strength between the oxide-oxide bonding is important for the improvement of reliability, and the bonding strength between the oxides should be sufficient enough to maintain the bonding, even if the force occurs in the opposite direction at the Cu-Cu interface after annealing. Among the diverse surface treatment methods, the plasma treatment is widely utilized, and this surface treatment can easily functionalize the required functional group [7-9]. Applying the plasma treatment to the oxide surface may strengthen the adhesion of the oxide interface by activating the surface with dense hydroxyl groups. Moreover, considering the low temperature (below 250°C) of Cu-Cu, the oxidation of Cu surface should be minimized even after the plasma treatment.

In this study, we realized 3D DRAM packages up to 16 stacks with daisy-chained HBM chips by adjusting various plasma treatment parameters including pressure, bias power, and gas type. Also, a modified single beam cantilever (SBC) method for measuring the bonding strength between the thin chips was developed, and we investigated the effect of plasma treatment on the characterized chip level bonding strength.

II. THE STRUCTURE AND PROCESS

The micro solder bump of conventional flip chip bonding and direct bonding of Cu-Cu are compared in Fig. 1. The conventional bonding structure is composed of solder bumps and gap fill materials at the joint gap. However, HCB involves the direct stack of wafer-to-wafer or die-to-wafer, with the space between the oxide surfaces approaching zero. The general process flow for D2W bonding is showed in Fig. 2. The oxide films deposited by CVD are planarized by utilizing CMP process on the bottom and top wafer. Next, the top wafer is coated with protective layer on the surface to protect from the contaminants, and the top chips are prepared from dicing. Then, surface activation including DI rinse is applied to a Cu patterned wafer to generate hydroxyl(-OH) group on the surface, and bonding is held consecutively in room temperature. Three types of condition are used and named Plasma A, B, and C with different bias power, pressure, and gas source. At this state, hydrogen bonding is formed by the silanol group of oxides, and bonded chips on the wafer are annealed. The dehydration condensation reaction between the oxides induces Si-O-Si covalent bonding , and the Cu Pads of bottom and top wafers are bonded by thermal diffusion of Cu atoms.

A. Oxide and Cu Surface Analysis

Fig. 3 shows the correlation between average -OH intensity and the contact angle according to different plasma condition. The amount of hydroxyl groups on the wafer surface is measured through time of flight secondary ion mass spectrometry (ToF-SIMS) depth profile, and the hydrophilicity of the surface is confirmed by the contact angle which is below 10°. The condition of plasma C indicates the highest -OH intensity, and this result leads to the lowest contact angle of the surface.

![Fig. 1. Cross section of conventional flip-chip bonding using (a) solder bump, and (b) Cu-Cu bonding of HCB technology](image)

![Fig. 2. D2W HCB Process including the preparation of top chip and bottom wafer, and bonding](image)

![Fig. 3. Contact Angle vs. Avg.-OH density in accordance with Plasma A (orange), Plasma B (grey), and Plasma C (sky blue)](image)
In D2W bonding, surface roughness is an important factor for bonding. The rough surface may be detrimental because particles will induce voids in the bonded surface. Also, smoother surface can realize larger real contact. AFM is applied to measure the surface roughness of the oxide and Cu PAD according to the plasma conditions in Fig. 4. The surface roughness values of oxide and Cu PAD according to the different plasma conditions (A, B, and C) are less than 1nm, and the condition of plasma C shows the smoothest surface.

B. Novel Characterization method of Bonding Strength

In case of D2W bonding, one of the important factors of the high quality oxide to oxide bonding is measuring the bonding strength between the oxide interfaces at the chip level. The common approaches for bonding strength is double cantilever method for wafer to wafer bonding strength at wafer level [10]. However, as the die thickness of the chip gets thinner for the multi stack applications, it is difficult to insert the tip between the wafers to measure the crack length between the two thin chips. Therefore, it is critical to develop a methodology to characterize the bonding strength at chip level for the improvement of the bonding quality of D2W bonding. To evaluate the bonding strength between the oxide interfaces, the first top chip is bonded on the bottom wafer. Then, the bonding is performed by shift bonding the second top chip to make a place for uniform load in Fig. 5(a). The fabricated samples are evaluated by modified single cantilever beam test. By measuring the crack length of ‘a’ from load-displacement graph, the bonding energy $G_c$ was calculated using the following equation [11]:

$$ G_c = \frac{P_c^2 da}{2b da} $$

Where $P_c$ is the critical load that was applied at the end of cantilever, ‘a’ is the crack length, ‘b’ is the width of the beam, and ‘C’ is the compliance of the beam. Fig. 5(b) shows the bonding strength according to the plasma conditions which are represented as A, B, and C. The bonding strength is highest (Avg. 2.8 J/m²) when plasma C condition is applied, and the highest -OH intensity may lead to stronger bonding.

Fig. 5. (a) Structure of the sample for measuring bonding strength and the single beam cantilever (SBC) structure, (b) the bonding strength (inset image: the exfoliated top chip and the bottom wafer after the SCB method), and (c) the adhesion force according to various plasma conditions (inset image: the measuring structure for adhesion force)

The top chip and the bottom chip are cleanly separated after measuring the bonding strength with SBC method in inset image of Fig. 5(b). Comparing between the condition of Plasma A, Plasma B, and C, the bonding strength of Plasma
A is lower than that of Plasma B, C. In case of non-reactive group, the Si\textsubscript{2}N bridging bond may degrade the bonding quality, because this site is considered as inactive to bond [12]. Fig. 5(c) indicates the adhesion force of the oxide surface according to the different plasma conditions, and this value is measured by atomic force microscopy (AFM). When the AFM cantilever tip gets close to the surface, the deflection of cantilever increased as the tip approaches to the surface [13]. As the AFM tip is loaded to a critical force value, cantilever is freed from the surface, which means the adhesion force between the tip and the surfaces. The condition of plasma C with high bonding strength shows the highest adhesion force. The oxide films treated by plasma A have the lowest bonding strength compared to oxide films treated by plasma B, C. The plasma treatment may form sufficient Si-O- dangling sites, which indicates that the surface is modified to a bonding favorable state, and this induced high adhesion force.

C. Demonstration of 16 stacked chips by optimized plasma

Modulating the thickness of Cu oxide is also critical to enhance the bonding strength of hybrid bonding. If the thickness of Cu oxide at the interface is thick, it will be difficult for the Cu PAD to induce grain growths at the Cu interface. The Cu oxide of Cu PAD is compared between the various plasma conditions in Fig. 6. The plasma condition C has the lowest Cu oxide thickness (Avg. 4.3nm) by optimizing the plasma parameter including bias power and pressure.

Fig. 6. The Cu oxide thickness on Cu PAD measured by TEM in accordance with Plasma (a) C, (b) B, and (c) A

Applying the optimized plasma condition and the previously optimized CMP and bonding technology, the 16 stacked package structure is successfully demonstrated in Fig. 7(a). When the annealing is proceeded, the upper and lower Cu PADS contact together through Cu diffusion at the interface, and the well closed Cu–Cu bonding is shown in the magnified cross-sectional image in Fig. 7(b). Also, the Cu diffusion and grain growth at triple points was observed at the Cu interface in Fig. 7(c).

IV. Conclusion

In this paper, we have successfully demonstrated that multi-stack D2W packages could be realized by optimization of the plasma treatment. Also, a modified single cantilever(SCB) method was developed for measuring the HCB bonding at chip level. This method helped to optimize the plasma treatment by characterizing the bonding strength at the interface, and improved the bonding quality and reliability of the HCB bonding. The high-OH intensity on the surface indicated more -OH groups on the surface after the condition of plasma C, and this led to enhanced bonding strength (Avg.2.8J/m\textsuperscript{2}) and adhesion force. Moreover, the lowest Cu oxide thickness induced full Cu diffusion at the interface with a triple point. This optimized HCB strategy promotes the development of 16-hi stacked D2W structures.

Fig. 7. A cross sectional SEM image of (a) 16 stacked D2W, (b) Cu-Cu bonding interface, and (c) TEM characterization of the bonding interface

References