Demonstration of a Wafer Level Face-To-Back (F2B) Fine Pitch Cu-Cu Hybrid Bonding with High Density TSV for 3D Integration Applications

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Abstract— We have successfully fabricated a 2-Layers Face-To-Back (F2B) test vehicle (TV) by combining fine pitch Cu-Cu hybrid bonding technology with high density (HD) TSV. Three different stacked structures, built on 300 mm wafers, are needed to achieve the F2B TV. There are different Cu damascene levels that simulate back-end-of-line (BEOL) layers commonly used in 3D integration. Morphological characterizations have been carried out and highlighted the integrity of the 3D structure. Furthermore, results of electrical tests on Kelvin and Daisy-Chain structures demonstrated a high connectivity. Kelvin and Daisy-Chain test structures are designed with either standard or fine pitch configuration (Pitch: 6 μm and 4 μm respectively) with hybrid bonding pad dimensions of 3 μm and 2 μm respectively. HD TSV dimensions are 1 μm in diameter and 10 μm in height.

Keywords—3D Integration, Hybrid Bonding, Wafer Level, 3-Layers, High Density TSV, Fine Pitch

I. INTRODUCTION

Nowadays, 3D vertical integration has become a key concept for overpassing Moore’s law. Since the semiconductor industry has almost reached its limits in terms of the smallest pattern that is possible to reach, alternatives solutions have been developed in order to sustain the growing demand in adding new functionalities with increasing I/O density and data processing speed combined with low power consumption.

Focused on these common objectives, alternatives multi-stacking interconnection technologies have been developed for several years now, either at the wafer or at the die level. Among them, the most popular is Cu-Cu hybrid bonding with integrated TSV.

Hybrid bonding at the wafer level is widely used now for high-density memory and CMOS Image Sensors (CIS) [1] devices. Whereas, it is typically used at the die level when we have to deal with heterogeneous integration challenges such as, for example, III-V materials.

Focusing on hybrid bonding at the wafer level, a lot of works have been done and published worldwide ranging from material studies to functional TV with 3-Layers [2-4] and even 4-Layers structures [5-].

CEA-Leti is also working on hybrid bonding both at the wafer and at the die level for years now. At the wafer level [8-12], we are currently developing with industrial partners a Cu-Cu hybrid bonding based technology combined with HD TSV in order to achieve a 3-Layers functional device (Fig. 1.a) that firstly involved the development of a 3-Layers TV with high interconnection density (Fig. 1.b).

In this paper, we will describe the fabrication of an intermediate 2-Layers TV which is faster to achieve compare to a 3-Layers while bringing together the most important technological building blocks for this kind of multilayer chip : Cu-Cu hybrid bonding with a least one wafer having high density TSV. After structure and process flow description, morphological results are reported as well as electrical resistance evaluations and experimental performances on Kelvin and Daisy-Chain structures. A high connectivity is finally demonstrated.

Fig. 1. (a) 3-Layers final device scheme. (b) 3-Layers TV cross-section.
II. TV STRUCTURE DESCRIPTION AND FABRICATION

As it was pointed out in the introduction, the 3-Layers structure, being so complex, was not directly fabricated. We decided to start with a more simplified structure as an intermediate step to the 3-Layers TV. Due to the high number of fabrication steps, the characterization and electrical results of the 3-Layers TV will be presented soon.

A. F2B TV main structure dimensions

The F2B TV is described in Fig. 3.g. The structure is fabricated with three different 300 mm wafers using oxide/oxide and Cu-Cu hybrid bonding.

The via diameter is 600 nm, the width of bonding pads are 2 μm and 3 μm. The pitch depend on the type of Daisy-Chain, it is 4μm (fine pitch) and 6 μm (standard pitch) while TSV dimensions are 1μm in diameter and 10 μm length (Aspect ratio = 10:1).

B. F2B TV fabrication process

The F2B TV starts with the fabrication of three different tiers in parallel. The first one, the tier 1, is formed by 3 metal levels: a line level (MZ), a hybrid bonding via (HBV) level and a hybrid bonding metal (HBM) level (Fig. 2.a). Tier 2 is formed by a metal line level (M1) encapsulated by dielectric layers (Fig. 2.b) whereas, the tier 3 has only a thin oxide layer (Fig. 2.c). M1 and MZ represent the first and the last BEOL levels respectively. However, for the sake of simplicity, the M1 and MZ dimensions of the F2B TV are larger than typical production dimensions.

The first assembly is a direct oxide/oxide (Ox/Ox) bonding, between tier 2 and tier 3 (tier 2/3), see Fig. 3.a. After bonding, the tier 2 is thinned down to 9 μm (Fig. 3.b) in order to fabricate the 1x10μm TSV (Fig. 3.c). Then, a damascene level is made on the top of TSV to create bonding pads (HBM pads, Fig. 3.d). Face-to-back hybrid bonding is made between tier 1 and tier 2/3 (Fig. 3.e). The Silicon of tier 3 is then removed (Fig. 3.f). Finally, the passivation is opened in order to perform electrical tests (Fig. 3.g).

III. FABRICATION PROCESS INLINE CHARACTERIZATION

The F2B TV fabrication passed through different steps. In this paper, some of the most critical ones are characterized, such as Ox/Ox bonding, Silicon thinning and Cu-Cu hybrid bonding (HB).

A. First bonding: Ox/Ox bonding

After fabricating the tier 2 and tier 3, these two wafers are bonded in an EVG bonder tool after a Chemical Mechanical Polishing (CMP) process developed at CEA-Leti which guarantees a very low level of roughness (< 0.5 nm) and nanotopology (< 5 nm) for bonding. To evaluate bonding quality, Scanning Acoustic Microscopy (SAM) is used, and typical results are shown in Fig. 4.a. Darker areas are related to good bonded areas while lighter areas are associated to unbonded areas. The cross section in Fig. 4.b shows the Ox/Ox bonded stack achieved at this step.
B. Top Silicon wafer thinning

After Ox/Ox bonding, tier 2 was thinned down to 9 μm with two different grinding tools. 2D mappings of the top Silicon (Si) thickness for the thinning tool 1 and state of the art thinning tool 2 are presented in Fig. 5.a and Fig. 5.c respectively. Total Thickness Variation (TTV) of the thinned wafer obtained with tool 1 is 3.4 μm, see Fig. 5.b, while the TTV of the thinned wafer obtained with tool 2 is 1.2 μm, see Fig. 5.d. Even if it always better to lower the final TTV, it has been demonstrated that the TSV height variation has less influence than the TSV diameter on the final electrical resistance [13].

C. Second bonding: Hybrid bonding.

After the top Si thinning step, 1x10 μm TSVs were fabricated on the backside of the tier 2, see Fig. 2.c. Then, the hybrid bonding metal pads (HBM) were patterned on top of the TSVs. The complete stack after hybrid bonding is shown in Fig. 2.d.

Fig. 6 presents the SAM images of the Cu-Cu hybrid bonding with/without defects.

The first hybrid bonding trials had some unbonded areas (white areas in Fig. 6.a). After surface preparation improvement, the Cu-Cu hybrid bonding was optimized as shown in Fig. 6.b where full dark scan reveals that the two tiers are well bonded. The cross section achieved at this step is shown in Fig. 6.c. The wafers are aligned and bonded with an EVG GEMINI tool. Thanks to the Alignment Verification Module (AVM) of the bonding tool, we are able to reach a $|\text{mean value}| + 3 \sigma$ below 500 nm (see Fig. 7) which is compatible with the TV pitches.

In this paper, only the electrical results of the bonded wafers, shown in Fig. 6.a, will be presented.

IV. MORPHOLOGICAL RESULTS

After the Cu-Cu hybrid bonding, top Si wafer was removed. The FIB-SEM image of the final F2B TV structure is reported in Fig. 8.
The F2B stack is made of a metal line level (M1), a TSV level, two HBM levels, a HBV level and final metal level (MZ). The hybrid bonding interface is indicated by a dotted line.

According to figure Fig. 9.a, the contact between TSV and metal line level (M1) is good as we expected. Connection between TSV and HBM level is shown in Fig. 9.b.

Fig. 10 shows the HB interface (see dotted line) and the bottom of the F2B stack. The good bonding quality between the two HBM pads lead to a robust F2B TV structure.

V. ELECTRICAL RESULTS

A. Primilary resistance evaluation for Kelvin structures

An estimation of the Kelvin structure resistances is presented in TABLE 1. Based on the 2D and 3D representation, a standard pitch Kelvin structure (STD KEV) is formed of one TSV, two HBM pad (3x3 μm²), four HBV in parallel, as reported in Fig. 11.a and Fig. 11.b; while, the fine pitch Kelvin structure (FP KEV) is made of one TSV, two HBM pads (2x2 μm²) and two HBVs in parallel, as it is reported in Fig. 11.c and Fig. 11.d.

Perfect conditions are assumed for the evaluation of the Kelvin resistance i.e. no HBM pad misalignment, negligible contact resistances between the different metal levels, perfect 3D shapes except for the TSV part of which value was taken from [13].

B. Experimental results

The median resistances for the STD KEV and the FP KEV are 1.15 Ω and 1.64 Ω respectively (see Fig. 12). The main difference between the two structures is the via number per TSV (Fig. 11.b and Fig. 11.d). A shift is observed between STD and FP KEV as well as more dispersion for the last one. It suggests that via resistance contribution is higher than the expected evaluation (TABLE 1).

<table>
<thead>
<tr>
<th>Contribution of elementary component</th>
<th>STD KEV (Ω)</th>
<th>FP KEV (Ω)</th>
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<tbody>
<tr>
<td>HBV level</td>
<td>0.052</td>
<td>0.104</td>
</tr>
<tr>
<td>HBM level</td>
<td>0.014</td>
<td>0.030</td>
</tr>
<tr>
<td>TSV level</td>
<td>0.504</td>
<td>0.504</td>
</tr>
<tr>
<td>Total</td>
<td>0.570</td>
<td>0.638</td>
</tr>
</tbody>
</table>
The yield of these two Kelvin structures is close to 80%. The 20% die losses are related to the unbonded areas of the wafer as can be seen in Fig. 6.a. A better yield is expected with the next optimized bonded wafers (Fig. 6.b).

Experimental values are twice over the evaluated ones, shown in TABLE 1. Many factors could explain these results such as non-optimal electrical connectivity between the HBM pads at the bonding interface and between the different damascene levels (i.e. TSVs on HBM pads, HBVs on metal lines, etc.), or copper electrical property degradation within damascene levels. In order to quantify the impact of these assumptions, TEM and EDX analysis might be performed.

In Fig. 13, the resistance for standard pitch Daisy-Chains (STD DC) with different number of links is presented. There is only little dispersion between the different STD DCs. The number of STD DC links vary from 6 to 3240 links. The median resistance for a STD DC half link, roughly equivalent to a STD KEV structure, is 1.05 Ω whatever the chain length. It is in good accordance with the STD KEV median resistance (see Fig. 12).

The resistance of fine pitch Daisy-Chains (FP DC) is shown in Fig. 14 and there is little dispersion as for the STD DC. The number of FP DC links vary from 8 to 3240. The median resistance for a FP DC half link, roughly equivalent to a FP KEV structure, is 1.30 Ω. It is also in good accordance with the FP KEV median resistance (Fig. 12).

However, higher electrical resistances are obtained with Kelvin structures versus equivalent half link Daisy-Chain structures. The via and TSV densities are higher in Daisy-Chain than in Kelvin structures. It is well known that a same pattern diameter in a dense matrix becomes larger than an isolated one after etching. Knowing that the electrical resistance (R) strongly depends on via and TSV diameters (R ∝ 1/D^2), it could explain the lower values for Daisy-Chain versus Kelvin structures.

The median leakage current has also been measured (Fig. 15) and is slightly higher than 10^-6 A. These values mean that the isolation of the structure is not optimal and it can be explained by a discontinuous isolation liner at the TSV level [13]. This issue can be overcome by using ultra-conformal dielectric deposition techniques for the TSV isolation step.
high density TSV with either standard (6 μm) or fine pitch (4 μm). Hybrid bonding pad dimensions are 3 μm and 2 μm respectively. High Density TSV dimensions are 1 μm in diameter and 10 μm in height.

Morphological characterizations are performed in order to validate the whole 3D stacked structure. Good metal connection between the two hybrid bonding pads at the hybrid bonding interface has been demonstrated as well as good metal reconnection between HD TSV and M1 level hence demonstrating the high performance of the HD TSV fabrication process.

For the electrical characterizations, two different types of Kelvin and Daisy-Chains structures (up to 6500 half-links) have been reported. Our best results for the STD and FP Kelvin structures showed a median resistance of 1.15 Ω and 1.64 Ω respectively. These encouraging results are validated by the electrical measurements on STD and FP Daisy-Chains structures with a median half-link resistance of 1.05 Ω and 1.30 Ω respectively.

Following these good results on the F2B 2 layers test vehicle, the next step is to demonstrate the functionality of a 3-Layers TV with 2 hybrid bonding interfaces.

ACKNOWLEDGMENT

We would like to thanks Paul Besombes and David Bouchu for FIB-SEM images, Antonio Roman for the etching process development and Stéphane Moreau for its expertise in the analysis of electrical tests.

This work was supported by the French National Research Agency (ANR) under the “Investissements d’avenir” programs: ANR 10-AIRT-0005 (IRT NANO-ELEC).

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