Co-packaged Optics on Glass Substrates for 102.4 Tb/s Data Center Switches

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Abstract—Next generation data centers are challenged with the task of delivering increased bandwidth and data rates at manageable power consumption. Co-packaged optics offer a path forward by enabling significant power reduction when electronic and photonic chiplets are locally mounted on a packaging substrate. In this paper, we discuss a glass substrate solution where both optical and electrical connectivity can be fabricated using ion-exchange (IOX) waveguides embedded into the glass and low-loss electrical routing. Design aspects are discussed to support 102.4 Tb/s data center switch applications. Signal transmission between the ASIC and PIC is completed with a total of 5 metal layers utilizing fine-line signal routing separated by ground planes. Through glass vias (TGVs) provide both power delivery for the mounted components and data management connectivity. Low-loss evanescent coupling occurs between the waveguides embedded in the glass substrate and photonic chips with high-density silicon nitride optical IOs. This design enables low-cost assembly methods involving the pick and place alignment of optical components and offers connectivity with low-profile mechanical transfer (MT) ferrule based fiber connectors.

Keywords—glass, interposer, surface mount technology, multichip modules, optical waveguides, silicon photonics, connectors, optical coupling

I. Introduction

Next generation electrical devices require the pursuit of further performance gains whether these are higher bandwidth, denser I/O escape, lower latency, and lower power consumption for the task at hand. The backbone of any electronic device is the integrated circuit with performance improvements gained for each CMOS node size reduction. As improvements delineate from Moore’s law, other techniques have been developed such as the use of multicore processors, chiplets and heterogeneous integration and the implementation of optical architectures in electronic systems. These techniques continue to present unique challenges for device level interconnections which are especially relevant to data center and telecommunication networks.

The trajectory of networking switch generations has roughly doubled every two years with the current state-of-the art chips providing a switching bandwidth of 51.2 Tb/s [1]. It is expected that co-packaged optics will enter the testing and deployment stage at the next leap to 102.4 Tb/s. Using this as a guideline, the work presented in this paper sets out to develop the design criteria and structure for a glass-based solution.

The basis of this work is an optoelectronic glass substrate which incorporates optical interconnects, electrical redistribution layers (RDLs), and through glass vias (TGVs) in a single package (Fig. 1). Both the high-capacity ASIC and the PIC would be connected to the RDL through electrical connections. The optical interface consists of an evanescent coupler between the silicon photonic chiplet and the glass waveguides integrated in the substrate. The glass waveguides are interconnected to optical fibers via an optical fiber array connector. The length of the glass waveguides could be extended all the way to the front panel to replace fiber fly-overs.

II. Device Components

A. Glass Waveguides

The optical connectivity portion is based on embedded waveguides in the glass. These are produced using a thermal ion-exchange batch process where the replacement of ions in the masked substrate results in a local refractive index change. Multiple sheets can be processed in parallel for scalability and lower cost. Alkali containing glass wafers (150 mm diameter) were first processed with a lithographic mask to outline the waveguide pattern. Next, a thermal ion-exchange step is completed to embed silver ions into the substrate. The mask is then removed, and the substrate undergoes a second thermal ion-exchange step in a sodium salt solution to finalize the waveguide shape. These waveguides have previously been shown to perform at 1310 nm with propagation loss of 0.08 dB/cm [2].
B. Low-profile Fiber Connector

To overcome packaging limitations of pigtails for CPO, a novel low-profile fiber connector was developed for mating an array of optical fibers with the glass waveguide substrate along the edges which are laser cut with optical end-face quality. A high-precision high-precision MT-ferrule in combination with two guide pins with latching features directly placed in mechanical alignment trenches on the glass substrate (see Fig. 2a) enable a four-fold smaller form factor compared to a standard MPO-16 connector and solder reflow compatibility. A mated 16 fiber connector to the edge of a glass substrate is shown in Fig. 2b. For 102.4 Tb/s with FR4 optical interfaces, each glass substrate requires four of such connectors on each side of the glass substrate. Due to the small width, connectors can be placed with 8.5 mm pitch. For a connector with 5 N spring force for physical contact, the average connector loss was 0.72 dB including 0.3 dB mode-mismatch between IOX glass waveguides and single-mode fiber.

![Fig. 2. (a) Guide pins with trench assembled to the glass and (b) mated connector.](image)

C. Evanescent PIC Coupler

Evanescent couplers were designed for SiN waveguides for glass with integrated IOX waveguides. The photonic chip is composed of U-shaped waveguide loopbacks with 250 μm pitch for testing. For demonstration of the optical interface, the passive optical chip was aligned by fiducials and Vernier patterns and flip-chip bonded with index-matching adhesive with a bondline of 1μm or less. Insertion loss due to evanescent patterns and flip-chip bonded with index-matching adhesive passive optical chip was aligned by fiducials and Vernier for testing. For demonstration of the optical interface, the composed of U-shaped waveguide loopbacks with 250 μm pitch glass with integrated IOX waveguides. The photonic chip is between IOX glass waveguides and single-mode fiber. Connector loss was 0.72 dB including 0.3 dB mode-mismatch.

![Fig. 3. Test vehicle layout consisting of a 50 mm x 50 mm glass substrate with 4 PICs mounted along one side of an ASIC. Low-profile fiber connectors mate along a laser cut edge near the PICs.](image)

III. Test Vehicle Design & Fabrication

For the specified 102.4 Tb/s switch, one potential design would include 16 optical modules each with 6.4 Tb/s. Electrical delivery requirements are expected to approach 224 Gb/s according to the CEI-224G specification [3] which is currently in development. Optical module requirements are based upon the work by the Co-packaged Optics Collaboration Joint Development Forum which released a product requirements document (PRD) for 3.2 Tb/s CPO modules [4]. The document is based upon a 16-module solution for a 51.2 Tb/s switch using co-packaged optic. The discussed modules can support 400GBASE-DR4 with a total of 32 Tx/Rx channels operating at 106G which is compliant to CEI-112G-XSR specification. Extrapolating for a 102.4 Tb/s package is done by using the 3.2 Tb/s PRD optical module pad layout definition and number of ports as a baseline but allow for operation at the future 224 Gb/s specification to achieve the required bandwidth. Electrical connectivity in the document is completed by LGA pins on a 0.6 mm pitch while this work uses pads at a 180 μm pitch. The optical module footprint is comprised of 25 x 34 pads (rows x columns). Routing from the ASIC to the PIC is required by 64 differential traces for each PIC.

To support this design, a test vehicle was developed based upon the signal routing needs along one package edge (Fig. 3) where the PIC is co-located near the ASIC and the ASIC hosts the SerDes functionality. This uses a 25 mm x 25 mm ASIC and 4 optical modules along one edge and allows for a 50 mm x 50 mm overall footprint that can be easily replicated (x4) on a 150 mm glass wafer and maintain a reasonable package size acceptable for demonstration. IOX waveguides route from the PIC locations to the glass edge where optical connectors would attach. Photonic test chips were fabricated with 800 electrical bonding pads of 50 μm rectangular size on a 180 μm pitch (Fig. 4). The layout is based upon the 3.2 Tb/s PRD form factor with 25 rows along the chip edge facing the ASIC. Bare spaces were made available in the electrical footprint to allow for placement of the ASIC upon two pedestals which extended from the cavity floor and aid in leveling the PIC during attachment. PICs of approximately 5 mm x 10 mm were selected for this study. For simplicity, the ASIC test chip utilizes the same pad pitch of 180 μm as the PIC. For a 25 mm x 25 mm chip, the pad outline consists of 137 rows/columns and a total pad number of 18,753 with some corner pads removed to accommodate fiducial marks. Both the PIC and ASIC test chips were designed with a custom daisy chain pattern for verification of later bonding steps. With the selection of a PIC layout based upon the 3.2 Tb/s PRD module, a pad pitch of 180 μm, and the usage of 64 differential electrical lines. During a design analysis it was found that the signal transmission lines could be routed using two layers with a line width of 10 μm. As in the 3.2 Tb/s PRD document, the signal layers are separated by ground planes.
Fig. 4. PIC layout with area of 5 mm x 10 mm for opto-electrical integration.

Fig. 5 shows a geometry of an edge coupled differential stripline and stack-up of the RDL layer. It consists of three GND layers, two signal layer and four dielectric polymer layers with dielectric constant of 3.2 and tangent loss of 0.033. The differential stripline was initially designed based upon a line/spacing of 10/20 μm, a copper thickness of 5 μm, and a dielectric thickness of 5 μm. To optimize the RDL layer, a parametric study was performed by varying the line width (w=4-13 μm), line spacing (s=15-25 μm), and Cu/substrate thickness (t=3-5 μm and h=5-15 μm respectively). Fig. 6 shows the simulated differential S-parameters with different geometrical parameters. The polymer substrate thickness and line width dimensions are critical for good impedance matching. Especially, a polymer substrate thickness is most dominant on an impedance matching, and 15 μm was optimum. Results also showed improvement with a narrower line width while the line spacing had little influence. The copper thickness could also be reduced with a value closer to 3 μm found to be optimal. The line width is dependent on process yields which are currently targeting 10 μm production.

Fig. 5. Geometry of the differential stripline and RDL layer stackup.

The geometry of the initial and optimized striplines was applied on a subsection of the designed RDL layout with a total of 32 differential striplines (16 layers at upper and bottom signal layer each) with the soldering pads as shown in Fig. 7. To verify performance for current 112 Gb/s PAM4 communication standards, the single differential stripline with initial design conditions ([L/S=10/20 μm, h=5 μm, t=5 μm]) were evaluated against optimized conditions [L/S=10/20 μm, h=15 μm, t=3 μm]. The simulations were performed at 0.05~56 GHz with a symbol unit interval (UI) of 17.8571 ps, T-rise/T-fall time of 20/80% and a Nyquist frequency of 28 GHz. The optimized stripline shows an insertion loss of -2.6 dB at 26GHz and opened eye diagram unlike the initial design (Fig. 8).

Fig. 6. Simulated S-parameters (S11, S21) of the edge coupled stripline with different geometrical parameters: line width (top left), line spacing (top right), polymer thickness (bottom left), and copper thickness (bottom right).

Fig. 7. Geometry of the RDL layer showing signal lines routed between PIC and ASIC.

Fig. 8. Simulated S-parameters (S11, S21) and eye diagram of the initially designed (top right) and optimized (bottom right) RDL layer.
Using the guidance from the simulation results, an electrical layout was developed to support Copper routing with 10 μm line widths between the PIC and ASIC. Since the design encompasses multiple layers as a minimum of 512 signal lines plus power/ground interconnections, commercial electronic design automation (EDA) software was used for the auto routing features. Signal routing was completed using Cadence software to auto-route the electrical traces from PIC to ASIC. Signal lines are divided into two layers and each differential pair includes a tear-drop shaped signal pad surrounded by a ground via cage to improve signal integrity.

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IV. Conclusion

This paper presents an integrated optoelectronic glass interposer architecture to support advanced applications such as a 102.4 Tb/s data center switch. This approach uses a glass substrate consisting of embedded IOX waveguides and electrical routing fabricated within a cavity. The current focus has been upon the uppermost redistribution lines which allow for high-speed electrical connectivity between the ASIC and photonic modules while TGVs allow connectivity for power/ground and management lines. Optical connectivity consists of both evanescent coupling between the photonics modules and the embedded waveguides and off-package by edge coupled fiber connectorization. Applying these design concepts to a 102.4 Tb/s switch, a proposed test vehicle was described consisting of 64 differential lines per PIC with simulation studies to help identify a targeted RDL geometry. Ultrafine line and space down to 5 μm has been successfully fabricated within the glass cavity using a spray photoresist deposition process. Baseline fabrication processes have been demonstrated with process continuation into dielectric deposition techniques and multilayer buildup.

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References