A Scalable Heterogeneous AiP Module for a 256-Element 5G Phased Array
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Abstract—This paper presents design and integration considerations of a scalable 24 – 30 GHz 256-element phased array antenna module consisting of four 64-element tiles. We employ a heterogeneous integration approach to enable the effective and efficient integration of multiple ICs, bandpass filters, splitters, combiners, and decoupling capacitors in a multi-layered organic substrate which also integrates the 64 dual-polarized antenna array. The paper introduces and addresses technical challenges that arise in the heterogeneous integration of such large mmWave antenna-in-package (AiP) designs: 1) system architecture and functional partitioning among multiple technologies to enable performance and scalability, 2) design of the power delivery network to reduce supply modulation of mmWave active circuits, and 3) tiling considerations to preserve antenna performance when scaling to large antenna array modules. The proposed hetero-

geneous integration approach is validated by 360◦ radiation and beam scan measurements demonstrating beam scan across ±70◦ in E- and H- planes in both polarizations.

I. INTRODUCTION

Advanced millimeter-wave (mmWave) packaging is an interdisciplinary research field requiring innovation across the stack to support applications including 5G mmWave communications [1]–[3]. Silicon-based mmWave phased array front end systems enable large low-cost phased arrays with accurate beam control to overcome the high path loss at mmWave and mitigate interference challenges [4]. Recently, the high data rate requirements and cost pressures of 5G technology have motivated the co-integration of heterogeneous dies and passive components in an antenna-in-package (AiP) [3].

Consequently, the design of modern large-scale mmWave modules entails the integration of antenna arrays and multiple components in diverse technologies within a limited space. Such an implementation also results in complex signal and power delivery routing in a limited number of layers and presents challenges in both module and system design. In this paper, we introduce a 256-element transceiver phased array antenna module designed on a multi-layered organic substrate, as shown in Fig. 1. We focus on three key challenges: heterogeneous integration aimed at optimizing power, performance, and area (Section II); design, modeling and characterization of the power supply network (Section III); and the integration of multiple antenna-array tiles into a unified module (Section IV). Characterization results are presented in Section V to validate the proposed heterogeneous integration approach.
ICs to perform the active circuit signal amplification and frequency translation, (b) liquid crystal polymer (LCP) based filter and combiner/splitter chips to perform passive signal conditioning, and (c) surface mounted discrete capacitors for supply decoupling. All components are assembled on a single SLC substrate that also integrates 64 dual-polarized (dual-pol) antennas to create a phased array tile. The 64-element scalable phased array module/tile, as shown in Fig. 2, consists of nine SiGe BiCMOS ICs (one frequency conversion IC, or FC-IC, and eight beamformer ICs, or BF-ICs), two LCP-based 4:1 combiner/splitters and two LCP-based band-pass filters (BPFs), all attached to a package with integrated antennas. The module is suitable for the tiling approach first proposed in [8] and uses a high level functional partitioning approach similar to [9], [10]. The LCP-based filter (similar to that described in [11]) placed between the FC-IC and the BF-ICs not only improves spur rejection in the transmitter (TX) mode but also provides image rejection in the receiver (RX) mode. Moreover, the modular design enabled by these stand-alone filters provides a convenient hardware swap option to achieve operation in different 5G bands – the same wideband BF-IC and FC-IC with different antennas and filters produces module variants that can support the different frequency band requirements (i.e., n257/n258/n261 for 5G NR) in different geographies.

For scaling to larger phased arrays, the IF signals from each module’s FC-IC are combined/split at the board level when they are tiled to form larger phased arrays. The details of the BF-IC architecture and key circuits are discussed in [7] while details of the FC-IC architecture and design considerations are discussed in [10]. Each BF-IC comprises 16 TRX front ends (FEs) (8 FEs per pol). The eight BF-ICs in the 64-element tile contribute 128 FEs that support the 64 dual-pol in-package antennas. As described in [7] and [10], the active circuit blocks are designed to specifications that enable superior in-band performance such as TX efficiency and output power in TX mode, and RX noise figure and linearity in RX mode. Moreover, this superior performance is maintained across different 5G bands in different parts of the word using the hardware configurability enabled by the modular heterogeneous integration strategy adopted for this design.

Needless to say, beyond the system architecture and IC designs, the antenna performance and implementation play a critical role towards determining the performance of mmWave phased arrays. The AiP design and implementation in this work involves a careful balance between (a) non-radiating functions such as mechanical support for BF-ICs, FC-IC, LCP components and decoupling capacitors as well as RF, DC, and digital interconnects between them, and (b) antenna performance. Antennas need to achieve broad antenna radiation patterns to enable a wide beam scanning range in both E- and H-planes and in both polarizations, as well as provide uniform performance independent of physical location so as to eliminate the need for calibration. Moreover, since mmWave dual-pol phased array modules rely on a high density AiP implementation, the designs need to comply with high-volume manufacturability rules and account for array scalability. For low cost and high density AiP integration, a standard SLC process is chosen to meet the above-mentioned challenging requirements.

Fig. 3 shows the AiP stackup and the unit-cell antenna structure used in this design. Unlike most prior mmWave designs which are based on patch or Yagi antennas [12]–[15], this work uses magneto-electric dipole (MED) antennas. MED antennas were first introduced in [16], and have recently attracted wide attention because of their symmetric radiation patterns, high isolation between H- and V-pol ports, and relatively wider bandwidth than patch antennas [11], [17]–[20]. In this work, we implement and demonstrate MED antennas for the first time in silicon-based phased arrays.

Along with the MED antenna, design and layout considerations include antenna element spacing, feed lines, tile spacing, and package functionalities. For dual-pol applications, high port electrical isolation is a critical requirement. Although the MED antenna achieves good isolation between its input H- and V-ports, it is important to maintain this isolation throughout the rest of the package and at the ICs. The high H/V isolation is maintained in this design by physically separating the H/V signal paths from the IF I/O to the BF-IC antenna ports. Furthermore, all of the RF signal connections between the ICs and LCP components, and all of the antenna feed line connections between the BF-IC ports and the antennas, are separated between H- and V-pol avoiding any crossing points. A re-mapper block in the digital core swaps H/V registers, thus virtually creating the mirror design, instead of using separate physically mirrored ICs. As a result, the phased array module can operate without calibration, making it easier and less expensive to deploy and maintain. The module is also designed such that all antenna elements have the same feed line length from the radiators to the antenna ports on the bottom of the module. For calibration free operation, it is critical to also match the signal paths all the way from the IF I/O port to each
antenna port. Thus, at the 256-element board level, shown in Fig. 4, only four LO signals and four IF signals need to be matched. In addition to the matched feed line lengths along the entire chain, the routing in the application board helps to maintain symmetry.

III. MODELING AND CHARACTERIZATION OF POWER DISTRIBUTION NETWORK

The 256-element phased array antenna module that consists of four 64-element tiles utilizes four voltage domains for the BF-ICs and FC-ICs; two of these are digital supplies while the other two domains supply analog circuits. One of the supplies, the 1.5-V domain, feeds the power amplifier (PA) on the BF-ICs. The presence of power supply noise and signal dependent power supply modulation can potentially have a notable detrimental effect on the TX error vector magnitude [21], [22]. This section covers the design of the 1.5-V power supply on the package substrate and PCB, as well as the influence of an imperfect power delivery network (PDN) on the supply noise that is detected at the IC nodes.

A PDN’s main goal is to provide a low-noise and consistent voltage to the active devices. To analyze the power supply in the AiP assembled on the PCB, this section introduces a modeling methodology, simulation results, and measurement results of voltage variations at the BF-IC 1.5-V supply node.

Fig. 5 depicts the model of the 1.5-V PDN on the PCB and package. The 1.5-V power is supplied at the power pin strip and delivered through the metal shape (light blue) on the PCB toward the AiP module. The need for allocating multiple voltage domains in the limited number of layers in the PCB and package precludes the utilization of ideal power planes that maintain low inductance, high capacitance, and thus good power integrity. Through the ball grid array (BGA) between the PCB and AiP module, the power is supplied to the PDN in the AiP module (light green), where two BF-ICs share a PDN metal shape. The current is then supplied to individual BF-IC front ends through 200-μm pitch solder bumps.

To lower the impedance and suppress the noise at the BF-ICs, eight 1-μF decoupling capacitors per BF-IC are surface-mounted on the other side of the antenna (see Fig. 1). The addition of the surface mounted capacitors imposes assembly challenges – the total number of components assembled on the AiP includes 78 components: 9 SiGe-based ICs, 4 LCP-based passive chips, and 64 capacitors. However, as described below, the addition of the capacitors results in significant improvement of the power supply fidelity.

The PDN modeling and simulations were performed in an electromagnetic field solver (Fig. 5) – the PDNs of the PCB and the AiP module are modeled and simulated separately and the extracted models were cascaded during analysis. Fig. 6 plots the simulated cascaded PDN impedance at a solder ball on one of the eight BFICs flip-chipped on the package substrate, with and without eight 1-μF on-package decoupling capacitors placed adjacent to individual BFICs.
Placing decoupling capacitors between the voltage domain and reference ground at different levels (i.e., PCB, package, and IC) is a common approach to mitigating power supply noise. The PDN impedance at 50, 100, 200, and 400 MHz, which are the data bandwidths of interest in 5G-NR FR2, was lowered by a factor of $2 – 5 \times$ by the addition of the on-package decoupling capacitors.

Measured results at the data bandwidths for various back-offs from OP1dB are shown in Fig. 7. The standard deviations of the voltage variations at 100 MHz with 8-dB and 12-dB back-off from OP1dB improved by more than $10 \times$ while those at 50 MHz reduced by $2 – 4 \times$.

**IV. Tiling Considerations for Array Scaling**

Phased array antennas often consist of hundreds, even thousands, of elements to meet the link budget requirement. A practical and widely used approach to realize very large phased arrays is to tile many small or medium sized phased array modules [4], [23]. Small or medium sized phased array modules that deliver good performance are relatively easy to design and to manufacture with good yield.

However, while tiling phased array modules, one needs to be mindful of gaps between tiles that often get introduced. At mmWave frequencies, tile gaps ranging from a few hundred microns to several millimeters can represent a significant fraction of the wavelength, thus affecting phased array performance, including radiation and beam scan [24], [25].

To analyze the gap effect on phased array performance, we focus on the array factor (AF), assuming isotropic antenna elements for the analysis. Note that the overall beam pattern can be obtained by multiplying the AF with the element pattern [26]. For simplicity, we consider a 1-D array, equivalent to analyzing the beam steering of the major plane of a 2-D array. Fig. 8 shows a 1-D phased array consisting of $N$ phased array tiles with $M$ elements at $d$ spacing and with a gap $\delta$ between...
Fig. 8. Illustration of a linear (1D) array consisting of \( N \) subarrays with \( M \) elements per subarray.

The AF can be expressed as

\[
AF = \sum_{n=0}^{N-1} \sum_{m=0}^{M-1} a_{nm} e^{-jkm\sin\theta} e^{-jkn(Md + \delta)\sin\theta},
\]

where \( a_{nm} \) are the array excitation coefficients.

To study how the gap \( \delta \) effects array side lobe levels, we will assume

\[
a_{nm} = e^{jkm\sin\theta} e^{jkn(Md + \delta)\sin\theta}.
\]

The resulting array factor can be calculated as:

\[
AF = \frac{\sin \left( \frac{Md + \delta}{2} \right) \sin \left( \frac{Nk(Md + \delta)}{2} \psi \right)}{M \sin \left( \frac{2\psi}{2} \right) N \sin \left( \frac{k(Md + \delta)}{2} \psi \right)},
\]

where \( \psi = \sin \theta - \sin \theta_0 \). And the first null angles will be at

\[
\theta_{FN} = \sin^{-1} \left( \frac{\pm 2\pi}{Nk(Md + \delta) + \sin \theta_0} \right).
\]

Fig. 9 shows the array factors for the cases with \( N = 6 \) 1-D subarrays, where each subarray has \( M = 8 \) antenna elements, and element spacing \( d = 0.5\lambda \) with gaps \( \delta = 0, 0.5, 1.0 \) and \( 1.5\lambda \), respectively. The increase in the gap, \( \delta \), lowers the first null location (since the array’s physical size has been increased), causes non-monotonic side lobe levels, and an increase in the side lobe level values. This increase is due to the misalignment between the grating lobes of the tile array factor and the zeros/nulls of the subarray array factor [27].

The effect of tile size on the level of the highest side lobe is shown in Fig. 10. For the Fig. 10a, we assume that the array contains two tiles with each tile containing 4, 8 and 16 elements. The larger number of elements per tile lowers side lobe level of the largest sidelobe. The tile gap \( \delta \) in the 256-element module presented in this paper is 2.55 mm, which is 0.25\( \lambda \) at 28 GHz. When the gap is present, the side lobe level is elevated by 1.39 dB relative to the scenario where no gap exists, as shown in Fig. 10a. This derivation is consistent with the measured result (i.e., \( \sim 1 \) dB degradation) reported in [7]. Fig. 10b assumes a 64-element array with different combinations of subarrays and tile sizes. Throughout the study discussed in Figs. 9 and 10, an increase in the gap tends to increase the array side lobe levels and reduce the overall aperture efficiency. Besides gaps between tiles, the tile size is also critical to the array performance.

Fig. 11 shows the effect of a 0.25\( \lambda \) gap on the array side lobe levels and beam direction errors for a 1-D array with two tiles and eight elements/tile as the beam is scanned. Fig. 11a indicates that the array side lobe level does not change much when the beam is scanned if the array elements are excited with the proper phases (eq. 2). However, if the array elements are excited with the phases calculated for an array without considering the gap (uniform array), the beam direction will have errors as shown in Fig. 11b. For the 1-D array here with 0.25\( \lambda \) gap, the beam direction error will be less than 5° for up to 60° beam scans, also consistent with the 5° measurement for the uncorrected beam reported in [7]. The beam direction error is corrected in the design by the on-chip beam calculator introduced in [28].

To show the validity of the 1-D array gap analysis, Fig. 12 shows the comparison of the array radiation patterns when scanning at 0°, 30° and 60° using a 1-D array with two tiles and eight elements/tile. These 1-D AF results are compared to the 256-element array measurement; the analytical results (labeled Sim) agree well with the measured results (labeled Meas) in Fig. 12. Specifically, the measured main lobes and first side lobes agree with the analytical results.
V. BEAM SCANNING CHARACTERIZATION

This section demonstrates the 64-element module beam scanning performance measured across the entire 360° in a plane. The measurement setup is shown in Fig. 13. The module, which is attached to the application board, can be rotated over a −180° to 180° range. The module is tested in Tx mode and placed in the far field at a 3 meter distance from a receiving horn antenna. The tests are performed at 28 GHz for co-pol and 28.4 GHz for cross-pol in the n257 band. The use of the slightly-different frequencies enables measurement of both co and cross polarizations simultaneously with a spectrum analyzer. In this experiment, it is also valuable to check spurious emission power levels and frequencies caused from LO, IF co-pol, and IF cross-pol. This test is accomplished by setting LO to 25 GHz and IF to 3.0 GHz for co-pol and 3.4 GHz for cross-pol, respectively. For the radiation measurements, the module is rotated from −180° to 180° with 1° increment. The resulting measurements show the beam direction, gain, complete side lobe levels and front-to-back ratio.

Fig. 14 shows the uncalibrated measured beam scan within −70° to 70° range for the −180° to 180° range module rotation for the horizontal (H) and vertical (V) polarizations in the E-plane (EP) and H-plane (HP) for the co-polarization (CP in color plots) and cross-polarizations (XP shown using the black color). The 64-element phased array module exhibits reasonable scan performance without calibration considering that the module is very compact as is necessary for tiling. As seen in the measured results, the main beams begin to split starting from ±60° toward the horizontal directions on the E-plane. This splitting is due to the fact that the module ground plane is notably small (necessary for scaling), causing hard-boundary diffraction at the ground plane edges (first order diffraction) in the E-plane. Note that for the H-plane, we get soft-boundary diffraction (second order diffraction) [29] resulting in a wider scan performance without beam splitting. When the ground plane is very large, the edge diffraction will be weak. Integrating multiple tiles to form a very large phased array will also reduce the edge diffraction effect since the antennas in the center region of the phase array play a dominate role as observed in [7]. If the module is used standalone, dummy antennas or absorber materials around the module can also be applied to improve the radiation patterns on the E-plane. Fig. 15 shows that the absorber materials around the module on the PCB improve the E-plane radiation patterns at large scan angles.

VI. CONCLUSIONS

This paper outlined the scaling and integration considerations for a large-scale phased array antenna module comprising 256 dual-pol transceiver elements, operating at a frequency range of 24 – 30 GHz, and consisting of four tiles, each with 64 elements.

We employed a heterogeneous integration solution to enable efficient and effective integration of multiple components, such as SiGe BiCMOS beamformer and frequency-conversion ICs, LCP-based high quality-factor filters and combiners, ceramic-based decoupling capacitors, and in-package antennas, in a multi-layered organic substrate.

We introduced and addressed the technical challenges that arise in the heterogeneous integration of mmWave AiP modules with an emphasis on 1) our integration approach to reduce
cost and improve performance using hardware reconfiguration of the overall architecture, 2) modeling of the power delivery network and reduction of power supply noise using in-package surface-mounted decoupling capacitors, and 3) the phased array scaling issues related to the gaps between the tiles that produce beam scan direction and sidelobe errors.

We also presented 8 × 8 dual-polar phased array module radiation pattern measurements in the −180° to 180° range (first-of-a-kind) with beam scans in the −70° to 70° range for both polarizations. The measurement results demonstrate superior beam forming and beam scanning performance and low power supply noise for the critical PA supply. Coupled with low cost manufacturing choices and hardware reconfigurability options, the module exhibits the potential for use in large base station phased arrays for 5G mmWave communications applications.

Fig. 14. 360° radiation and beam scan measurement results: the co-polarizations in colored-plots at 28 GHz, cross-polarizations in black color at 28.4 GHz. (a) H-pol H-plane for co-polarization, V-pol E-plane for cross-polarization, (b) H-pol E-plane for co-polarization, V-pol H-plane for cross-polarization, (c) V-pol H-plane for co-polarization, H-pol E-plane for cross-polarization, (d) V-pol E-plane for co-polarization, H-pol H-plane for cross-polarization

Fig. 15. The effect of the absorber material on the module E-plane radiation patterns. Left: Module not surrounded with the absorber showing distorted E-plane radiation patterns at large angles. Right: Module surrounded with absorber showing no distortion in E-plane radiation patterns

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REFERENCES


