Supercarrier Redistribution Layers to Realize Ultra Large 2.5D Wafer Scale Packaging by CoWoS

S. Y. Hou
Taiwan Semicondutor Manufaturing Company, Ltd
Hsinchu, Taiwan
SYHOU@tsmc.com

Chien Hsun Lee
Taiwan Semicondutor Manufaturing Company, Ltd
Hsinchu, Taiwan
CHLEEC@tsmc.com

Tsung-Ding Wang
Taiwan Semicondutor Manufaturing Company, Ltd
Hsinchu, Taiwan
TDWANG@tsmc.com

Hao Cheng Hou
Taiwan Semicondutor Manufaturing Company, Ltd
Hsinchu, Taiwan
HCHOUB@tsmc.com

Hsieh-Pin Hu
Taiwan Semicondutor Manufaturing Company, Ltd
Hsinchu, Taiwan
HPHU@tsmc.com

***Abstract*— Interposer based 2.5D systems have gained popularity to integrate chips and chiplets of advanced logic and stacked memory of high bandwidth memory (HBM) for performance-oriented artificial intelligence (AI) high performance computing (HPC) systems. The size of the interposer is one of the key indices for this technology. At a given transistor density, a larger interposer area means the capacity to carry a higher number of transistors within a package, which directly contribute to the overall performance gain for technology advancement.**

In this paper, we propose and demonstrate a new CoWoS interposer structure to realize an unprecedented interposer area of ~4000 mm^2. This is achieved by a multiple layers of supercarrier redistribution layers (SC-RDL) at the backside of LSI (local Si interconnect) interposer of CoWoS-L. The SC-RDL's fan out to an area the same as the organic substrate so that the key technology challenges associated with interposer at this size range are greatly mitigated. These include the difficulty of oS (on substrate) assembly, C4 bump pitch scaling, package reliability margin, and high package coplanarity issues. The structure has been demonstrated on mechanical samples of a 91 mm x 91 mm package. Excellent package coplanarity and structure stability as checked by multi-reflow are reported. It also holds the potential to simplify the routing layers in the organic substrate by fanning out the IO's to cover the entire substrate. In addition to achieving the interposer dimension scaling continuously, the SC-RDL based CoWoS-L with the extended area also promises to accommodate more embedded passives and optical engines required in a CPO (co-packaged optics) structure.

Keywords—CoWoS, interposer, 2.5D, HPC, super carrier (SC) RDL, LSI, HBM, uBGA, COP, metal TIM

I. Introduction

In recent years, artificial intelligence (AI) developed rapidly and gained tremendous attention worldwide. In addition to the advancement of the software and algorithms, dedicated AI-centric chips with high processing throughputs to provide meaningful results in a timely manner are attributed for this trend. The most popular deep learning chips today are AI accelerators which integrate most advanced logic and memory chips in one package. To maximize the bandwidth and minimize the energy per bit between the logic and memory, a Si interposer with TSV (through Si via) is added between functional chips (or top dies in this specific configuration) and the package substrate, as shown in Figure 1. This structure is known as 2.5D package [1]. The number 2.5 denotes that, while the top die level are active chips/chiplets, this chip-on-wafer (CoW) module is not a true 3D (i.e., active on active) structure, since the interposer itself does not carry any functional circuits .

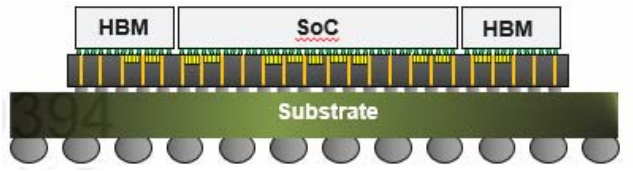
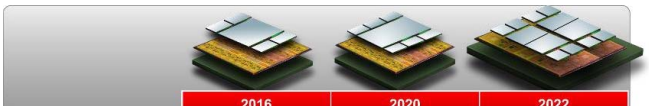


Figure 1. CoWoS-S provides high interconnect density for high-performance logic chiplets and high data bandwidth HBM

The continuous increase of interposer area is one of the main themes for CoWoS development road map to meet the overall performance improvement with time. This is a direct way to enable the integration of more active circuits, and is complementary with the transistor scaling pursued under Moore's Law. As shown in Figure 2, the interposer area has nearly doubled from 2016 to 2022. The logic top die technology also migrated from 16/12 nm to 5 nm. The number of HBM stacks have grown twice from 4 to 8, with a total memory capacity increase by four times, from 32 to 128GB.



	2016	2020	2022
Top die	N16/N12 SoC	N7 SoC	N5 SoIC
Max. Interposer Area, Reticle, mm^2	1.75X, ~1400	2.2X, ~1760	3.3X, ~2800
HBM Type	HBM2 @1.8 Gbps	HBM2E @3.2 Gbps	HBM3 @6.4 Gbps
Max. No. of HBMs/pkg.	4	6	8
Max. Memory Density, GB	32	96	128
Max. Memory BW, TB/s	0.9	2.5	6.5

Figure 2. CoWoS technology evolving with increasing interposer size and HBM memory density

2377-5726/23/$31.00 ©2023 IEEE
DOI 10.1109/ECTC51909.2023.00091

The fifth generation CoWoS with 3 reticle size (3x) [1] Si interposer (~2,600mm^2) with 4-mask stitched enhanced interposer has been developed, as shown in Figure 3 [5]. New, low thermal resistance TIM (thermal interface material) is applied to reduce thermal resistance between the die surface and lid. Embedded deep trench capacitor (eDTC, or iCap in ref. [5]) at a unit cell density of 320 nF/mm^2 is implemented in the Si interposer to boost the power integrity (PI).

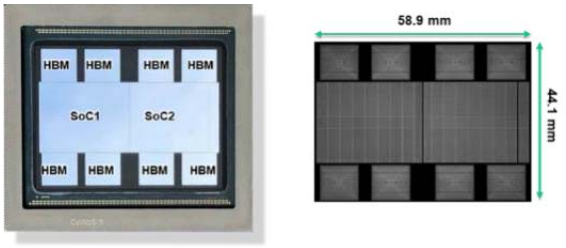


Figure 3. The Fifth Generation CoWoS with ~2,600 mm^2 (3x) Si interposer for two (2) SoCs, a (1) Chiplet and eight (8) HBM

2.5D packaging shares some of the most challenging issues or concerns in the field of advanced packaging. These challenges include:

- Interposer technology to deliver all the desirable interconnect, passives, and TSV features at a multiple-reticle size with a near-perfect yield.
- Complex warpage behavior of top dies (SoIC [8], SoC, and HBM) of different stacking schemes and material constitutions.
- An adequate assembly process to join CoW module on substrate at a near-perfect yield as the CoW warpage and C4 bump count increase, and C4 pitch scaling down.
- Control of the warpage for incoming substrates at extended layer count and size.
- Stringent package reliability challenge due to larger DNP (Distance to Neutral Point) and CTE (coefficient of thermal expansion) mismatch between CoW and organic substrate.
- Control of the package coplanarity of the final CoWoS SiP module to ensure subsequent surface mount process at PCB level.

For the interposer size up to 4x (~3300 mm^2), either Si interposer or reconstituted interposer (RI) may be employed [7]. RI with LSI (local Si interconnect) bears some advantage in the intrinsic yield due to relatively small LSI die size compared with Si interposer. The longer dimension of such an interposer is 65 mm, which is within the capability of die attach equipment. However, if we set the target on 5x to 6x (4000 to 5000 mm^2) interposer, the longer dimension of the interposer is estimated between 75 and 85 mm. At this dimension, the on-substrate assembly process becomes a technology bottleneck. Last but not the least, if the C4 bump pitch is reduced to 100 - 130 um, flux cleaning adds more difficulty in addition to the dimension of the interposer. Finally, the package coplanarity and component reliability will become extremely challenging. A solution to resolve all these issues and challenges are very desirable to enable a CoWoS solution at 6x (5000 mm^2) interposer.

II. CoWoS-L_6x SUPERCARRIER TECHNOLOGY

In this paper, we propose a new CoWoS integration solution to realize an equivalent interposer area up to 5000 mm^2 in a package. The new CoWoS scheme, CoWoS-L_6X, contains three main portions. 1. Top die layer (SoIC, SoC, and HBM) remains the same, except that a side mold is extended all the way to the edge of the package substrate. 2. LSI and SC-RDL (supercarrier redistribution layer), and 3. Simplified substrate. Top dies are connected to LSI and SC-RDL by ubumps, and the top die, LSI, and SC-RDL module is connected to simplified 3-2-3 substrate by uBGA, as shown as Figure 4.

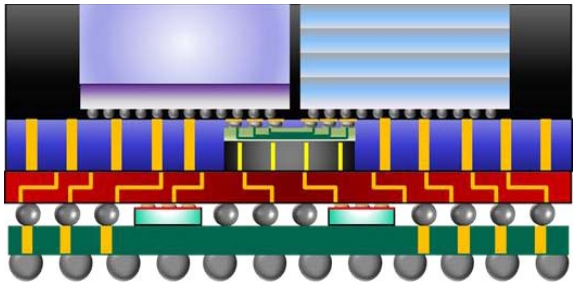


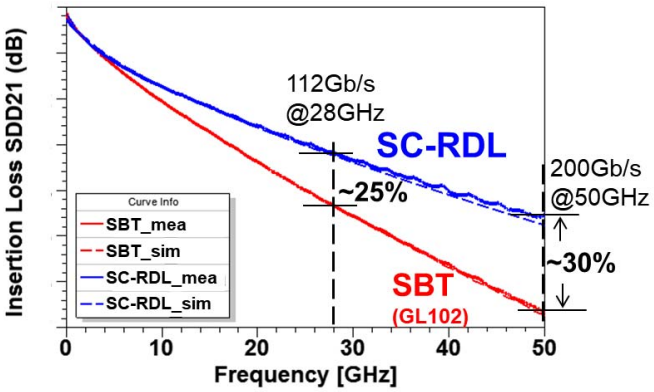
Figure 4. CoWoS-L_6x construction

Two different area dimensions are defined in this new structure. The interposer size is defined by the rectangle area enclosing the top dies with a 1 mm extension for each side. On the other hand, the new SC-RDL size is extended to the boundary of the entire package substrate. The SC-RDL layers comprise of seven RDL layers, one at frontside of LSI, and six at backside of LSI. The features included in LSI dies are the same as ref. [7] to meet various horizontal and vertical interconnect needs, as well as to provide embedded deep trench capacitors (eDTC). The 6 layers of backside RDL are processed with 11 um Cu line width and space over an innovative dielectric layer with low loss characteristic.

Several important merits for these SC-RDL's are noted. First, they assume the function of stress buffer to mitigate the stress due to differences of CTE between the top die Si chips and the organic substrate. This is extremely desirable in such a super large heterogeneous packaging system. Second, the superior electrical properties of SC-RDL can reduce the loading of buildup layers on the substrate. Consequently, substrate buildup layers can be minimized, which helps boost the yield of substrate, especially over 70 mm x 70 mm substrate size. Moreover, the insertion loss through wafer process Cu trace of RDL can be ~ 25% lower than that of organic substrate trace because of finer surface roughness (<100nm) provided by wafer process Cu trace shown in Figure 5. Third, these SC-RDL's widen the pitch differences between the top die (u-bump) and the substrate (typically C4 bump). That is, the u-bump pitch

[1] In this paper, one reticle size is defined as 830 mm^2, derived from the maximum patternable device area in a modern lithography scanner.

of SoC and HBM may be scaled to 35um or lower, while the pitch at the substrate interface can be much relaxed to reach the range of 400-500 um, like uBGA. This is very important to ensure the oS (on- substrate) yield for such a large package system. Furthermore, the total height of uBGA layer is controlled ~ 200um which can accommodate integrated passive device (IPD) also process separately in TSMC. To prove the concept of supercarrier redistribution layer structure, a mechanical test vehicle (TV) for CoWoS-L_6x was designed in two versions: TV0_1.6x (1.6x ret. top die with 3.8x ret. dummy silicon in top die layer) and TV0_4.8x (4.8x ret. top die), as shown in Table 1.



90Ω Impedance	Measured Insertion Loss		
	56Gb/s	112 Gb/s	200 Gb/s
SBT	1.0x	1.0x	1.0x
SC-RDL	~0.8x	~0.75x	~0.7x

Figure 5. Measured differential insertion loss comparison between SC-RDL and organic substrate (SBT) up to 50 GHz, Ref. [6]

A. TV_1.6x Mechanical TV demonstration

TV_1.6x mechanical TV was designed to prove the concept of supercarrier redistribution layer structure. The TV_1.6x comprises two SoC and four HBM2E for a total interposer size of 1.6x. An equivalent 3.8x dummy Si was added to mimic a 5.4x reticle (4500 mm^2) interposer. The SC-RDL and interposer module include six LSI's, one frontside (F/S) RDL and six backside (B/S) RDL. The entire SC-RDL area is the same as the substrate size at 91 mm x 91 mm. There are 45 IPDs (2.9 mm^2 each) embedded between SC-RDL layer and organic substrate.

The TV_1.6x has completed process feasibility check with good wafer warpage control. The warpage of TV_1.6x package with lid is excellent at 65 um at RT and ~150 um at 240°C, considering the large package size at 91mm x 91 mm (Figure 6). Physical cross-section of samples underwent six-time multiple reflows (MR6x, with conditions defined in Table 2) revealed no detectable defects by SEM at stress sensitive locations. Early reliability assessment with limited samples passed criteria and no abnormal C/TSAM images found post uHAST 396 hours (1 pass/1 total), TC-C 500 cycles (1/1), TC-G 850 cycles (2/2), and HTS 1000 hours (1/1), as shown in Table 2.

TABLE 1 TEST VEHICLE INFORMATION

Attribute	TV0_1.6x	TV0_4.8x
Interposer size	1.6x (w. 3.8x dummy Si)	4.8x
SC-RDL and Package size	91 mm x 91 mm	
Top die (Qty.)	SoC(2) HBM2E(4)	SoC(6) HBM2E(12)
Dummy die Qty.	8	0
SC-RDL	1 Front, 6 Back	
LSI Qty.	6	18
TIV	50um diameter, 100um pitch	
Substrate	3-2-3, 1.4 mm-core	
Ring/Lid	Lid	Ring
uBGA / BGA pitch	0.5mm / 1mm	

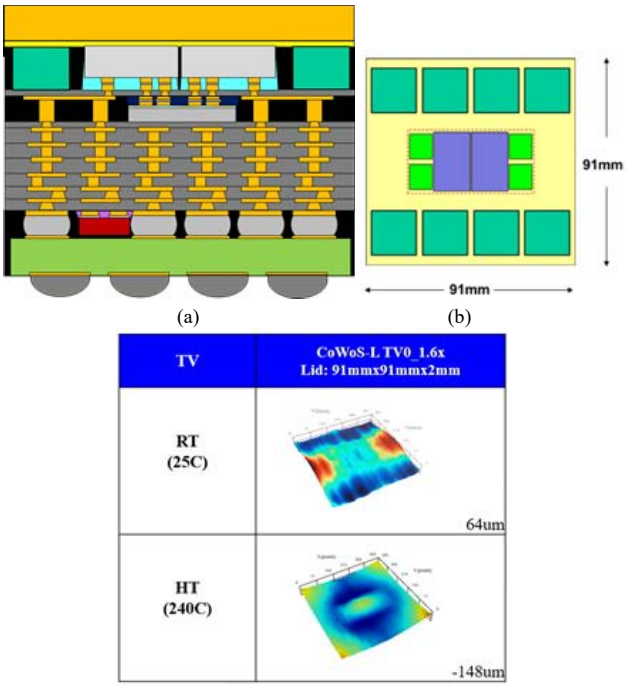


Figure 6. TV_1.6x package warpage (a) illustration cross-section and (b) Top view. (c) package warpage at room temperature and 240C.

TABLE 2. TV_1.6X TV EARLY RELIABILITY ASSESSMENT

ERA					
Item	MR6x	HTS	TCC	TCG	uHAST
	5x245C+ 1x260C	1000h	500c	850c	396h
Physical Result	Pass	Pass	Pass	Pass	Pass

B. *TV_4.8x Mechanical TV demonstration*

The TV_4.8x mechanical TV was designed to prove the concept of supercarrier redistribution layer structure with 4.8x ret. (~4000 mm^2) interposer area. The TV_4.8x comprises 6 SoC and 12 HBM2E at top die level. There are 18 LSI chiplets embedded in the SC-RDL, with 1 layer of F/S RDL and 6 layers of B/S RDL. The SC-RDL has the same size as the substrate at 91 mm x 91 mm. There are 45 IPDs (2.9 mm^2 each) embedded between the B/S RDL layer and 3-2-3 organic substrate. TV_4.8x has completed process feasibility check with good wafer warpage control. The warpage of TV_4.8x package with stiffener ring can be controlled within 200 um at RT and within 120 um at 240°C. Since the samples with stiffener ring exhibit good package warpage, it is a preferable option than the lid package, as shown in Figure 7. This is because the stiffener ring package can have heat sink directly contact the backside of top die and requires no TIM1. It not only saves the cost for TIM, but also eliminate the thermal resistance due to TIM1 for a more direct thermal dissipation. SEM cross section sanity checks on MR6x torture tested TV_4.8x samples again revealed no detectable defects at stress sensitive locations.

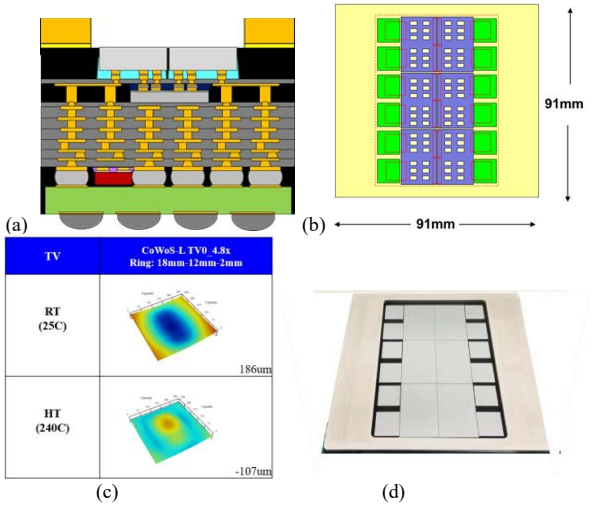


Figure 7. TV_4.8x illustration (a) Cross-section (b) Top view (c) Package with ring warpage at room temperature and 240°C (d) Package with ring picture

III. CONCLUSION

In summary, we demonstrated an innovative 2.5D CoWoS-L_6x package structure with a 4.8x ret. (~4000 mm^2) equivalent interposer mechanical TV. The samples possess well controlled warpage performance and passed package torture tests over limited samples. In this new structure, the six layers of backside SC-RDL's act as a thick stress buffer to mitigate the CTE mismatch between the large interposer and the substrate, and provides promising interconnect characteristics to partially reduced the buildup layers in the package substrate, which further helps to reduce the effective CTE of the substrate. The SC-RDL's also enabled uBGA at 400-500 um pitch as the interface between the CoW module and the substrate by acting as a pitch converter between the ubump pitch at top die side and the substrate interface. This makes the assembly process possible by conventional assembly tools. The demonstration of this work provides a promising path to realize wafer scale packaging based on CoWoS technology. In addition to achieving the interposer dimension scaling continuously, the SC-RDL based CoWoS-L with extended area also promises potential to accommodate chiplets over the entire package area by wafer level integration technology.

ACKNOWLEDGMENT

The authors would like to acknowledge the great collaboration and support from our R&D colleagues in tsmc, especially from the 3DIC Module-2 division, and 3DIC Integration division.

REFERENCES

[1] Lau, J.H.. "2.5D IC Integration". In: Semiconductor Advanced Packaging. Springer, Singapore, 2021. https://doi.org/10.1007/978-981-16-1376-0

[2] Hou, S.Y., Chen, W.C., Hu, C., Chiu, C., Ting, K.C., Lin, T.S., Wei, W.H., Chiou, W.C., Lin, V.J.C., Chang, V.C.Y., et al. "Wafer-Level Integration of an Advanced Logic-Memory System Through the Second-Generation CoWoS Technology". IEEE Trans. Electron Devices 2017, 64, 4071–4077.

[3] Liao, W.S., Chen, H.N., Yen, K.K., Yeh, E.H., Kuo, F.W., Yeh, T.J., Kuo, F., Jou, C.P., Liu, S., Hsueh, F.L., et al. "3D IC heterogeneous integration of GPS RF receiver, baseband, and DRAM on CoWoS with system BIST solution" Proceedings of the 2013 Symposium on VLSI Circuits, Kyoto, Japan, June 2013, pp. C18–C19.

[4] Yu, D. "TSMC Packaging Technologies for Chiplets and 3D". Proceedings of the 2021 IEEE Hot Chips 33 Symposium (HCS), Palo Alto, CA, USA, August 2021, pp. 47–56.

[5] Huang, P.K., Lu, C.Y., Wei, W.H., Chiu, C., Ting, K.C., Hu, C., Tsai, C.H., Hou, S.Y., Chiou, W.C., Wang, C.T., et al. "Wafer Level System Integration of the Fifth Generation CoWoS®-S with High Performance Si Interposer at 2500 mm^2". Proceedings of the 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, June 2021, pp. 101–104.

[6] Wu, Jiun Yi, Chen, Chien-Hsun, Lee, Chien-Hsun, Liu, Chung-Shi, Yu, Douglas C. H., "SoIS: An Ultra Large Size Integrated Substrate Technology Platform for HPC Applications", Proceedings of the 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, June 2021, pp. 101–104

[7] Hu, Yu-Chen, Liang, Yu-Min, Hu, Hsieh-Pin, Tan, Chia-Yen, Shen, Chih-Ta, Lee, Chien-Hsun, and Hou, S. Y., "CoWoS Architechture Evolution for Next Generation 2.5D System in Package", Proceedings of the 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, May 2023, (This conference)

[8] Chen, F.C., Chen, M.F., Chiou, W.C, Yu, Doug C.H., “System on Integrated Chips (SoIC™) for 3D Heterogeneous Integration”, Proceedings of the 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), May 2019, pp. 594–599.