Signal Integrity of 2-µm-Pitch RDL Interposer for High-Performance Signal Processing in Chiplet-Based System

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***Abstract*— Given the demand for advanced I/O interfaces, we have simulated eye diagram of 2-µm-pitch signal/ground lines based on coplanar topology and compared them with those of 4-µm-pitch signal lines based on embedded microstrip topology. Simulation showed that 2-µm-pitch signal/ground lines provide better signal integrity and thus enable high-performance signal transmission to achieve high-performance signal processing in the specification of HBM3 and UCIe1.0.**

Keywords—Chiplet, Heterogeneous, RDL, Interposer, 2.5D, HBM3, UCIe.

I. Introduction

Homogeneous and heterogeneous chiplet- and chip-based integrations are expected to break Moore's law of device scaling and achieve high-performance signal processing while increasing energy efficiency, in AI, graphics and other potential applications [1]. Fine-pitch Cu traces used as signal lines connecting chiplets/chips mounted on an interposer play a key role in high-performance signal processing because they must provide high signal integrity to meet the specifications of advanced I/O interfaces such as UCIe 1.0 (Universal Chiplet Interconnect Express) [2].

In ECTC 2022, we reported a large-scale redistribution layer (RDL) interposer fabricated using a 2-µm-pitch semi-additive process on a panel-scale glass carrier. Dry plasma etching to remove the barrier metal/Cu-seed layers enabled precise trace-width controllability in patterning Cu traces [3].

We have now simulated the signal integrities of 2-µm-pitch Cu traces based on the HBM3 and UCIe 1.0 interface specifications and compared them with that of a competitive interposer fabricated using a 4-µm-pitch semi-additive process.

II. Achievement of High Signal Integrity in HBM3

A. Signal Line Layout

High-speed signals are transmitted through Cu traces arrayed in two I/O sections corresponding to the physical I/O interface of the chips and in the middle section between them. Lengths of the signal line in the I/O and middle section were set to 2.6 mm (1.3 mm x 2) and 4.5 mm, respectively, so the total length of the signal line between HBM3 and logic chips was 7.1 mm (Fig. 1).

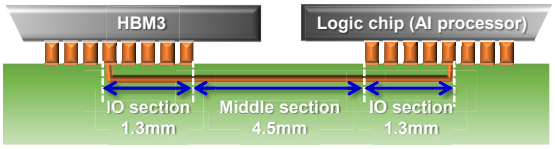

Fig. 1. Length of signal line consisting of both IO sections and middle section for specification of HBM3

With the HBM3 specification, 12 signal lines must be arrayed between 73 µm-pitch lands (via-lands) connecting to the I/O pads in the I/O section, if signal layers are supposed to be two layer [4]. This means that reducing the trace width enables the use of a coplanar layout (hereafter denoted as "GSG"), resulting in better routability (Fig. 2(a)). The GSG layout results in high signal integrity. A GSG topology can be patterned by using dry plasma etching technique based on semi-additive process previously reported. A signal line (1 µm wide) is sandwiched between ground line (1 µm wide) and spaced 1 µm from each ground. These dimensions were used in both the I/O and middle sections. We also investigated signal integrity of an additional topology in which ground line is shared by two signal lines (hereafter denote as SSG). To minimize cross-talk, neighboring signal lines were spaced as far part as 3.2 µm and 5.1 µm in the I/O and middle section, respectively (Fig. 2(b)). For both topologies, the 2-µm-pitch patterning of Cu traces can complete the interconnection of the signal lines between

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heterogeneous chips using just two signal layers, meeting with the I/O specification of HBM3. Limiting the number of signal layers as small as two layers effectively reduce the manufacturing cost as well as warpage of the RDL interposer. An increase in the warpage degrades bonding reliability between the heterogeneous chips and RDL interposer as well as RDL interposer and organic substrate.

Microstrip topology (hereafter denoted as "SSS") based on 4-µm-pitch signal lines is shown in Fig. 2 (c). In the middle section, signal lines are preferably arrayed over the entire I/O area width to reduce cross-talk. Thus, the spacing between neighboring signal lines is as much as 5.8 µm in the HBM3 interface.

In previous report, we checked thermal stability of 1K-via-scale daisy chain with a combination of 5-µm diameter via and 10-µm diameter land, by using thermal cycle test in which the number of thermal stressing cycle reached to 1000 cycles [3]. There was no failure after the stressing, meaning that the structure with the combination of the 5-µm diameter via and the 10-µm diameter land has a high thermal stability. From this, the land diameter was set to 10 µm.

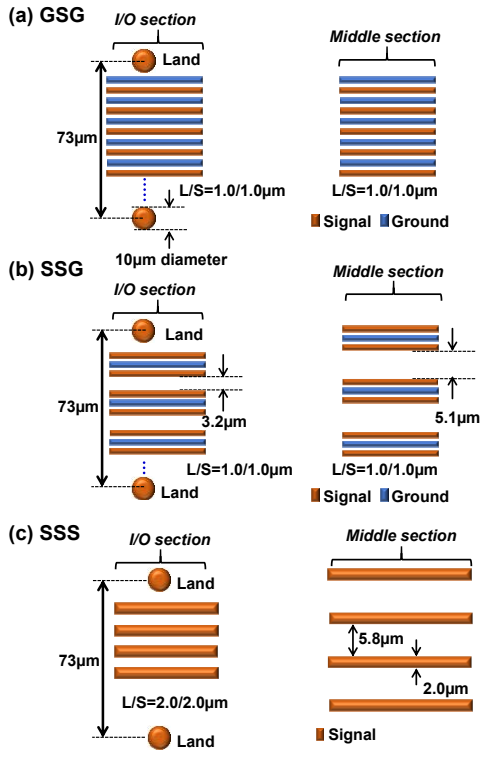

Fig. 2. Layout of signal line for topologies of GSG (a), SSG (b) and SSS (C).

Cross-sectional dimensions for the topologies of GSG, SSG and SSS used in the simulation are shown in Fig. 3. The dimensions for topologies of GSG and SSG are based on the minimum 2-µm-pitch (L/S=1.0/1.0 µm) patterning with aspect ratio as high as 3.0. The patterned Cu traces are covered with inorganic dielectrics to increase reliabilities [5, 6]. The topology of SSS was based on the minimum 4-µm-pitch (L/S=2.0/2.0 µm) patterning with aspect ratio of 1.0. The 4-µm-pitch patterning is frequently demonstrated in previous papers published by major OSATs and chip vendors [7, 8].

The topology of GSG and SSG are unacceptable for the 4-µm-minimum-pitch Cu traces (L/S=2.0/2.0 µm), if the number of signal layers are limited in two layers. Thus, the only viable option is embedded microstrip topology (SSS), in which 4-µm-pitch signal lines (2 µm wide) are arrayed on a ground plane layer in the I/O section.

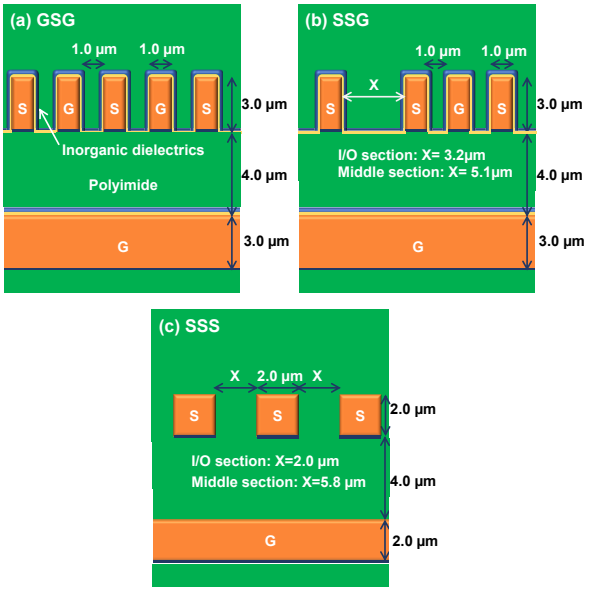

Fig. 3. Layout of signal line for topologies of GSG (a), SSG (b) and SSS (C).

B. *Pattering of 2-µm Pitch Signal/Ground Line*

A visual image of the in-process RDL interposer fabricated using panel level processing (300 mm x 400 mm) and its close-up image are shown in Fig. 4. The interposer was embedded with both the GSG and SSG topologies patterned with 2-µm-pitch Cu traces.

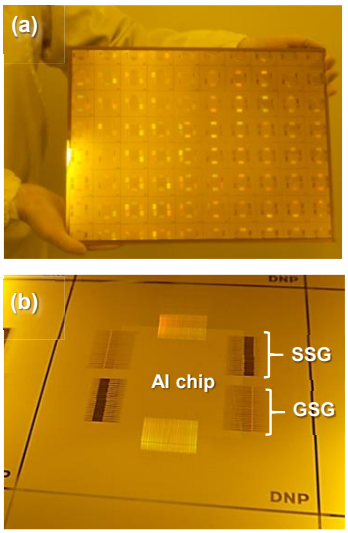

Fig. 4. Visual image of in-process RDL interposer using panel level processing (300 x 400 mm) (a) and its close-up image (b).

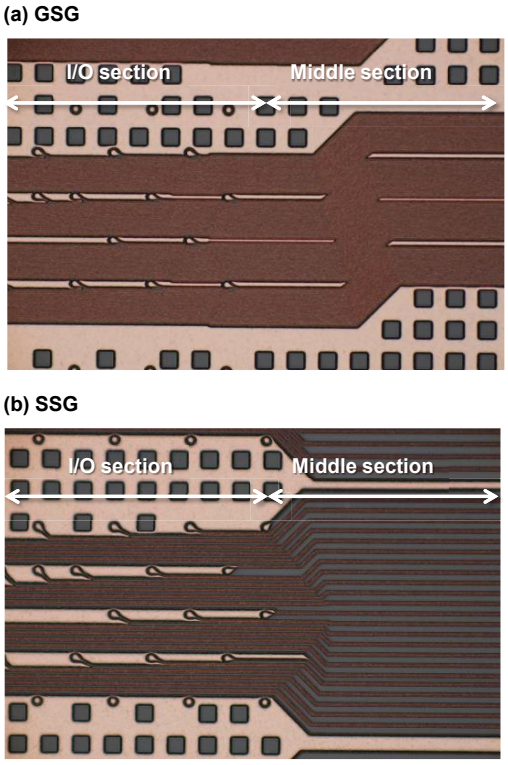

Fig. 5. Optical microscopic images of topologies of GSG (a) and SSG (b) in I/O and middle sections.

Optical microscopic images of topologies of GSG and SSG are shown in Fig. 5. For the GSG topology in the I/O and middle sections, a ground-level voltage for each ground line was supplied from the ground plane allocated under the signal layer, thorough the via. A signal and ground lines were alternately allocated through the 73-µm space between the lands, while their pitch was kept at constant of 2 µm in the I/O and middle sections. A height of the signal line was set to 3.0 µm to reduce conductor loss. Allocated ground lines could effectively reduce the cross-talk between the signal lines. For the topology of SSG, the entire width (vertical in the photo image) of signal/ground line arrays in the middle section is wider that in the I/O section to reduce cross-talk between neighboring signal lines.

The SEM images show the SSG topology in the I/O and middle sections (Fig. 6). A ground line was shared by two signal lines and 1 µm a way from both the signal lines. The spacing between neighboring signal lines is 3.2 µm and 5.1 µm in the I/O and middle sections to reduce cross-talk. On the basis of semi-additive process, we used anisotropic plasma etching to remove Cu-seed/barrier metal layers instead of wet chemical. This enables precise control of the trace width while keeping aspect ratio as high as 3.0. Controllability of the trace width and electrical isolation on the glass panel (300 mm x 400 mm) was demonstrated in previous report [3].

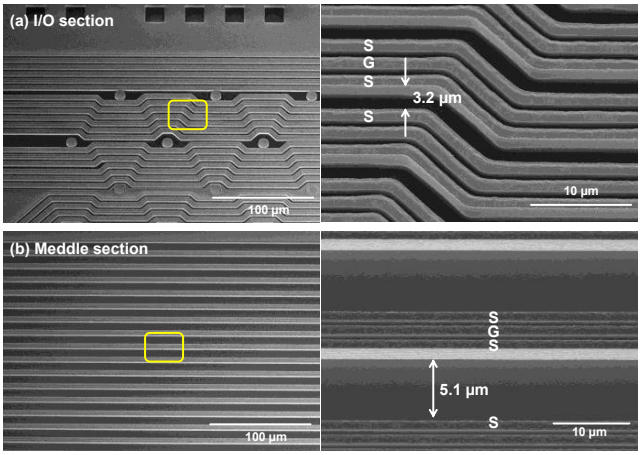

Fig. 6. SEM images of topologies of SSG in I/O (a) and middle sections (b).

C. *Signal Integrity in HBM3 Interface*

Although the waveform of the simulated eye diagram for the topology of SSS based on 4-µm-pitch signal lines did not across the keep out area (depicted with rectangle) defined by the specification of HBM3 at 6.4 Gbps, the wave form overshot and undershot the defined amplitude range of 0 to 0.4 V (Fig. 7 (c)). The observed overshoot and undershoot were both caused by cross-talk between neighboring signal lines. In addition, the waveform bordered the maximum peak amplitude for both the upper and lower sides (dotted line), indicating that the 4-µm-pitch Cu traces do not meet the HBM3 interface specification.

In contrast, the topology of SSG effectively reduced cross-talk thanks to the shield effect generated by the ground line, resulting in the overshoot and undershoot found in the topology of SSS being suppressed (Fig. 7 (b)). The topology of GSG further reduced cross-talk as well as jitter (Fig. 7 (a)). The waveforms of the topologies of GSG and SSG were away from the keep-out area enough, meaning that both topologies can provide high signal integrity in the specification of HBM3.

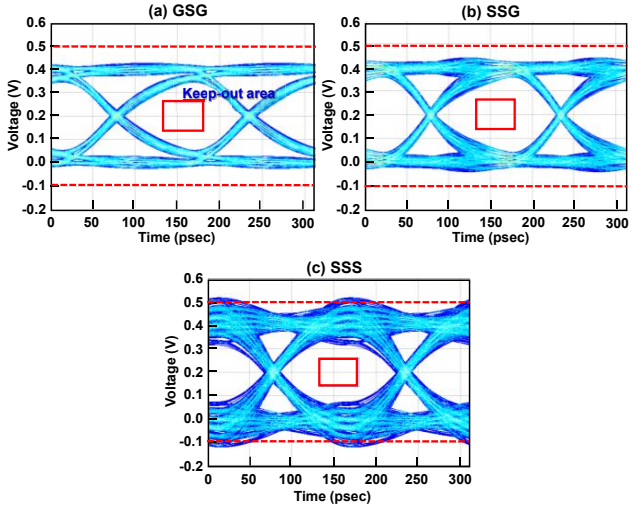

Fig. 7. Simulated eye diagram of topology GSG (a), SSG (b) and SSS (C) in specification of HBM3.

III. Achievement of High Signal Integrity in UCIe 1.0

A. Signal Line Layout

The specification opened in UCIe 1.0 is expected to provide standardization of chiplet-based communication for advanced packages. In the specification of advanced packaging, the required processing speed is ranged from 4 to 32 Gbps/line, which corresponds to the bandwidth density of from 1.0 to 10.5 Tbs/mm. On the basis of the specification of the UCIe1.0, we set signal line length between chiplets to 1.0 mm in the I/O sections (1.0 mm x 2) and 0.4 mm in the middle section, so the total length was 2.4 mm (Fig. 8). This is 20% longer that of the required signal line length/channel length between chiplets (2.0 mm) in the specification of UCIe 1.0.

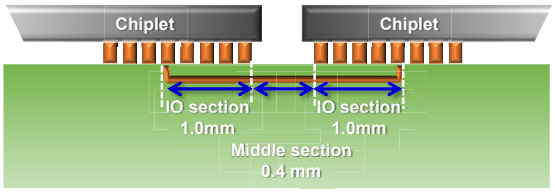

Fig. 8. Length of signal line consisting of both IO sections and middle section for specification of UCIe 1.0.

Fig. 9 is advanced package I/O land configuration based on UCIe 1.0, showing suggested design rule ratio. The 55 µm dimension is reference to a diagonal pitch. The horizontal is a multiple of 95 µm.

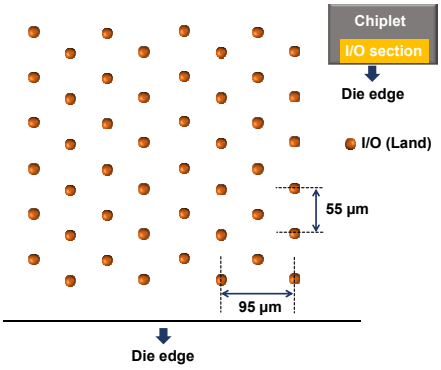

Fig. 9. I/O land configuration based on UCIe 1.0.

When the number of a signal layer is supposed to be two layers, 17 signal lines must be arrayed between 95-µm pitch lands. The topologies of GSG and SSG (minimum L/S=1.0/1.0 µm), of which signal line pitches are 4.0 µm and 5.5 µm, enable the allocation of 17 signal lines between them (Fig. 10 (a), (b)). To complete the allocation of all signal lines, two signal layers are also needed when applying the topologies of SSS (L/S=2.0/3.5 µm) (Fig. 10 (c)). Signal line pitch for the topologies is 5.5 µm.

In the middle section, signal lines can not be arrayed over the entire width of the I/O area to reduce cross-talk. This is different from in the case of the specification of HBM3. The signal line pitch must be kept at minimum of 5.5 µm for the topologies of SSG and SSS. This is because we can not use additional area generated by each land-array supplying ground-level or power-level voltage.

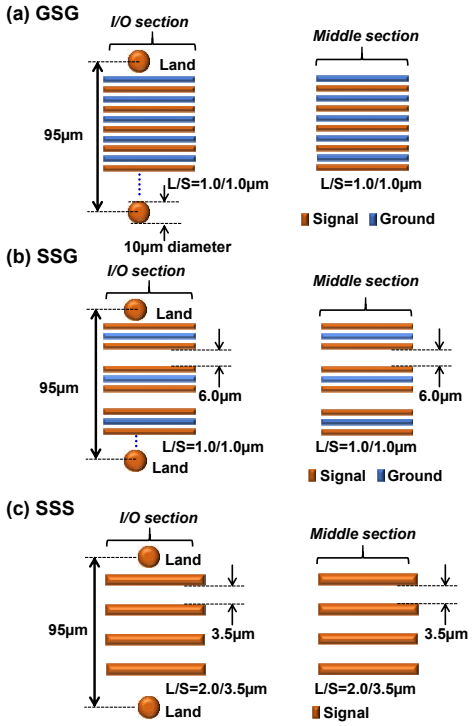

Fig. 10. Layout of signal line for topologies of GSG (a), SSG (b) and SSS (C).

Cross-sectional dimensions used in the simulation for the topologies of GSG, SSG and SSS are shown Fig. 11 (a), (b) and (c). Vertical dimensions for any topologies were the same ones shown in Fig. 3.

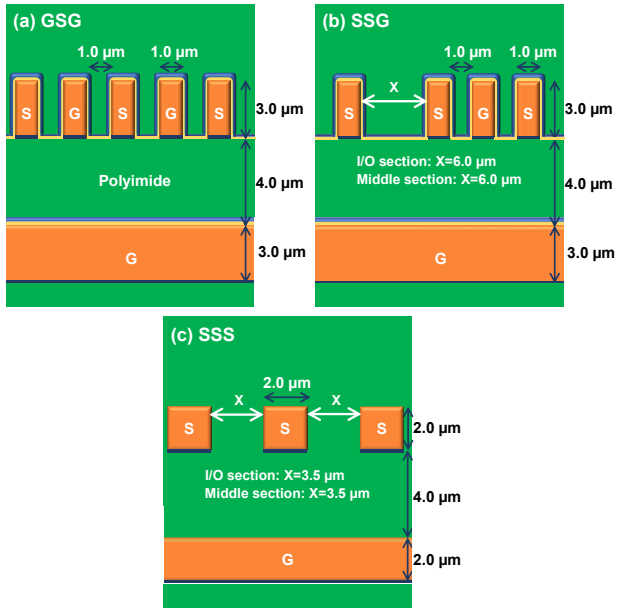

Fig. 11. Cross-sectional dimension of signal line for topologies of GSG (a), SSG (b) and SSS (C).

B. *Signal Integrity in UCIe 1.0 Interface*

We simulated eye diagram for the topologies of GSG and SSG on the basis of the specification of UCIe 1.0, comparing with that for the topology of SSS used as a benchmark.

The simulated eye diagram at signal transmission speed of 24 Gbps were shown in Fig. 12. The wave form for the topology of SSS crossed the left- and right-side keep-out (mask) area, meaning that the topology of SSS does not meet the specification of UCIe 1.0 at 24 Gbps (Fig.21 (c)). This is because cross-talk generated between the neighboring signal lines increased the amplitude variability of the wave form, resulting in degrading signal integrity.

The wave form for the topology of SSG did not cross the keep-out area, indicating a shield effect created by the ground line neighboring the signal line reduced the cross-talk (Fig.12 (b)). The wave form for the topology of GSG was away from the keep-out area enough (Fig.12 (a)). Both side ground lines neighboring the signal line greatly removed electromagnetic force generated around the signal lines. Both topologies of GSG and SSG met the specification of UCIe 1.0 at 24 Gbps. Even at the required maximum signal transmission speed of 32 Gbps, the topologies of GSG and SSG met the specification, as shown in Fig 13 (a) and (b).

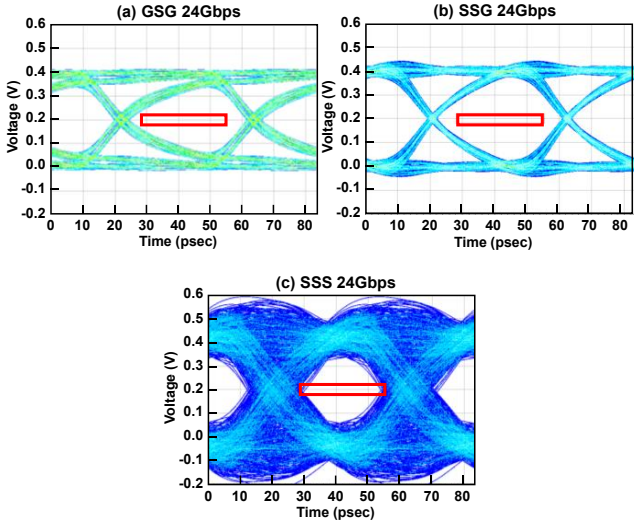

Fig. 12. Simulated eye diagram of topology GSG (a), SSG (b) and SSS (c) at 24 Gbps in specification of UCIe 1.0.

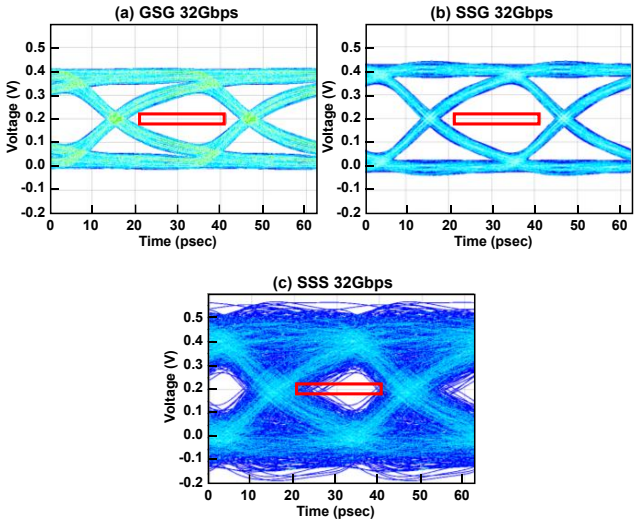

Fig. 13. Simulated eye diagram of topology GSG (a), SSG (b) and SSS (c) at 32 Gbps in specification of UCIe 1.0.

For the topologies of GSG, SSG and SSS, their available maximum signal transmission rate and needed number of signal layer to complete the interconnection of signal lines between chiplets are summarized in Table 1.

For the topology of SSS, the maximum signal transmission rate was 16 Gbps, and the needed signal layers are two layers. For the topology of SSG, the maximum signal transmission rate was increased up to 32 Gbps which is the highest one required in the specification, and the needed signal layer was two layers. For the topology of GSG, available signal transmission rate also reached to 32 Gbps.

Scaling down of Cu traces from 4.0-µm to 2.0-µm pitch and an application of the topologies of GSG or SSG to the signal transmission enable an increase in the signal transmission rate, while keeping the needed signal layers at as small as two layers.

TABLE I. AVAILABLE MAXIMUM SIGNAL TRANSMISSION RATE

Topology	Minimum L/S	Signal line pitch	Number of signal layer	Maximum transmission speed
GSG	1.0/1.0 µm	4.0 µm	2 layers	32 Gbps
SSG	1.0/1.0 µm	5.5 µm	2 layers	32 Gbps
SSS	2.0/2.0 µm	5.5 µm	2 layers	16 Gbps

IV. CONCLUSION

Simulation based on the specification of HBM3 and UCIe 1.0 showed the topologies of GSG and SSG based on 2-µm pitch patterning of signal/ground lines provided much better signal integrity, compared to that of the topology of SSS based on 4-µm pitch patterning of signal lines. In the specification of UCIe 1.0, by using the topologies of GSG and SSG, we achieved signal transmission rate of as high as 32 Gbps. This is the maximum one required in the specification. The reduction in

cross-talk generated by allocating the ground line between the signal lines greatly increased the signal transmission rate. In addition, for the topologies of GSG and SSG, we could complete the interconnection of signal lines between chiplets in just two signal layers. This greatly reduces manufacturing cost as well as a reduction in warpage of RDL interposer. If the topology of GSG is based on the 4.0-μm pitch patterning of Cu traces, the needed signal layers are increased up to four layers. This increases a warpage of the RDL interposer, resulting in degradation of reliability of bump connection between the RDL interposer and mounted chips. The increase in signal layer also causes manufacturing cost, which degrades competitiveness against Si interposer, in terms of high-volume mass production. Demonstrated anisotropic plasma etching to remove Cu-seed/barrier layers enabled a precise control in patterning 2-μm pitch Cu traces while keeping an aspect ratio as high as 3.0. This etching technique is expected to be useful for RDL interposers corresponding to the advanced I/O interfaces.

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