A New Adhesive for CoW Cu-Cu Hybrid Bonding with High Throughput and Room Temperature pre-Bonding

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***Abstract*—In this report, a new approach to high throughput, low-temperature chip on wafer hybrid bonding processes by using a unique adhesive is described. In our process, a bonding layer consisting of cured adhesive and slightly recessed Cu pads is fabricated on the chip surface, and the chip is bonded to another bonding layer consisting of SiO_2 and Cu pads fabricated on the target wafer. The chip is pre-bonded to the target wafer under compression for 1 second at room temperature by contacting the adhesive and SiO_2. By using the slight film shrinkage of the adhesive in the Cu-Cu bonding process, the two facing Cu contact and compressed. As a result, batch annealing process without chip compression becomes possible. Experimental results for the proof of our process are reported.**

Keywords—3D stacking, heterogeneous integration, chiplet, Cu-Cu hybrid bonding, adhesive, chip on wafer

I. INTRODUCTION

To address the growing demand for the evolution of high-performance computing devices, innovations in 3D stacking technology for logic and memory chips are required, in addition to continuous improvements of transistor scaling technology [1]. 3D stacking of homogeneous chips such as DRAM chips and 3D stacking of heterogeneous chips such as SRAM, core, and analogue chips can drastically improve computing performances (memory capacity, computing power, and power consumption) without some of the issues faced with transistor minimization (increased cost of circuit design and manufacturing, decreased chip yield, etc.). In current 3D stacked devices, chips are bonded using solder micro-bumps and epoxy-based adhesives. Minimization of the bonding electrode pitch is being vigorously researched in order to achieve higher bandwidth, higher speed, and lower power consumption signal communication between chips. Cu to Cu hybrid bonding with alternative dielectrics is a key technology for interconnecting chips with pitches less than 10 μm.

There are many reports on hybrid bonding using inorganics such as SiO_2, SiCN, and SiN. Some of the advantages of processes with inorganics are high throughput and room temperature pre-bonding of chips. One of the challenge is the chip bonding yield loss due to organic contamination and Si particles on the bonding surface after dicing [2-3]. As the number of stacked chips increases, as in high bandwidth memory, the impact of chip bonding yields is expected to become more significant.

Other approaches have explored organics such as polyimide and BCB. Since the modulus of organic material is much lower than that of inorganic materials, the void size becomes smaller than that of inorganic materials if particles of the same size are present on the bonding surface. Problems with organic polymers are thermal sliding and polymer extrusion from the edge of the chip during thermal compression bonding (TCB) due to polymer flow. A serious problem for organics is the coefficient of thermal expansion (CTE) mismatch between organics (typically 70-80 ppm/K) and Cu (17 ppm/K). Large organic CTE prevents Cu-Cu bonding if the bonding surface is flat after CMP. In conventional method, the bonding surface with protruding Cu (typically tens of nm) is prepared by CMP. Pre-bonding of the chips is then performed at high temperature (typically 250-350 ºC), then two facing Cu contact first and the two thermally expanded organics contact with each other. This technique requires a heating and cooling processes, which reduces chip bonding throughput (tens of seconds). Additionally, there is concern about deep oxidation of adjacent Cu pads on the target wafer.

To overcome the drawbacks of inorganics and conventional organics, one of the authors have developed a new adhesive (MA) [4-6]. MA is pre-bondable to SiO_2 at RT and permanently bondable after baking at 150 °C. The viscosity of MA is negligibly small, so there is no thermal sliding or no polymer squeezing from the chip corners after bonding. It is also showed that the low elastic modulus of MA (1 GPa at 250 °C) suppresses void formation due to particles on the bonding surface. In this work, a new approach for high-throughput and low-temperature Cu-Cu hybrid bonding by using MA is described.

Fig. 1 shows a standard chip on wafer process by using MA. First, a fine-pitch Cu pattern is fabricated on a Si wafer by the semi-additive method (SAP). After spin coating of a precursor solution of MA on it and curing at 200 °C for 1 h, a MA film is formed. After CMP, a flat bonding surface with Cu dishing (approximately 10 nm) is prepared. After separating the wafer into chips, the MA coated chips are pre-bonded to the target wafer at room temperature by contacting the MA to the dielectric of the target wafer. The compression time is 1 second

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per 1 chip and the pressure is 0.2 MPa. TCB or annealing without compression is applied for Cu-Cu bonding. At this stage the MA shrink slightly and the two Cu contacts and are compressed. Then, a stacked device is created.

II. FUNDAMENTAL PROPERTIES OF MA

MA was developed for back end of line interlayer dielectric applications. MA is a front end process compatible material due to its good purity level. In this study, 2 types of MAs were used. TABLE I shows the material properties of MAs. MA-0200 is soft material, and MA-1200 has the lower CTE and the higher T_g. Both materials have high thermal decomposition temperature according to the 5% weight loss temperature. In TABLE I, CTE was measured using a spectroscopic ellipsometer with a heating stage. A 20 mm × 20 mm square Si chip with a 700 nm thick MA film was placed on a heating stage in N_2. The MA on Si chip were pre-baked at 350 °C for 1h, and it was cooled to RT. Then, the stage was heated from 30 °C to 150 °C and the MA film thickness was measured every 10 °C. CTE was calculated from the change in film thickness from 30 °C to 150 °C. The elastic modulus at RT was measured by the nanoindentation method. Glass transition temperature (T_g) was measured with a differential scanning calorimetry.

A. Bonding strength of MA

The bonding strength of MA was measured. In this experiment, MA-0200 was spin coated onto a 4 inch Si wafer and cured at 200 °C for 1h under N_2 ambient with atmospheric pressure. The thickness of MA-0200 was 1 µm. The surface roughness (Ra) of MA was 0.5 nm. MA coated Si wafer was stacked at RT with a bare Si wafer having surface natural oxide (SiO_2). The bare Si wafer was UV-O_3 cleaned before the stacking. After applying a point load to the stacked wafer center, the two wafers were bonded. The creation of the bonded area over the entire area at the wafer to wafer bonding interface was measured by an IR camera. As reported in our previous works,[4-6] MA is spontaneously bondable under point loading. Therefore, near zero stress bonding can be realized by using MA. This allows stacking of very thin or mechanically fragile chips.

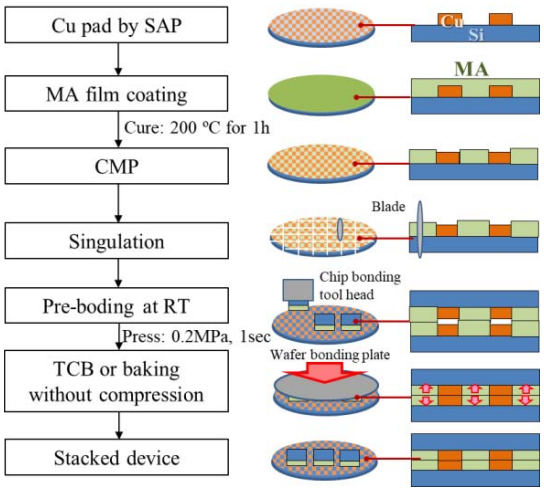

Fig. 1. Chip on wafer standard process by using MA. At the TCB or baking process MA shrinks slightly then the two Cu contacts and are compressed.

TABLE I. MATERIAL PROPERTIES OF MA

Type of MA	*MA-0200*	*MA-1200*
Coefficient of thermal expansion at 30-150 °C	*100 ppm/K*	*60 ppm/K*
Elastic modulus at RT	*6 GPa*	*6 GPa*
5% weight loss temperature	*>400 °C*	*>400 °C*
Glass transition temperature	*170 °C*	*>400 °C*

Fig. 1 shows bonding strength as a function of baking temperature. Here, baking was performed at 50-400 °C under N_2 to increase the bonding strength. The bonding strength was measured by Maszara method [7]. With no treatment before wafer stacking, the bonding strength between MA and SiO_2 was 0.1 J/m^2 at RT. Bonding strength increased with increasing baking temperature. MA is permanently bondable to SiO_2 after baking at 150 °C for 1 h if the criterion for permanent bonding strength is 2.5 J/m^2, which corresponds to the fracture energy of bulk Si. The baking temperature (150 °C) for permanent bonding is considerably lower than that (300-400 °C) for plasma activated SiO_2 to SiO_2 bonding [8]. Almost the same bonding strength was obtained between MA-0200 and SiCN, SiN, and MA-0200 itself.

It was found that the bonding strength at RT can be significantly enhanced by plasma treatment to MA-0200 before stacking the wafers [9]. The bonding strength was at the permanent bond level as shown in Fig. 2. This RT permanent bond has great potential for near zero thermal stress chip or wafer stacking applications. However, in this work, plasma activation was not used because the bonding strength without plasma activation is sufficient even for multi-chip stacking [10].

MA-1200 without plasma treatment has the similar bonding strength as MA-0200 without plasma treatment. It is pre-bondable at RT and permanently bondable with SiO_2, SiCN, and SiN after baking at 150 °C for 1 h under N_2 ambient.

The postulated bonding mechanism of MA is described below. For polyimide, BCB, and polybenzoxazole, these polymers is bondable above their T_g. At temperature above T_g the polymers interdiffuse with each other [11]. Permanent bonding is then made. The postulated MA bonding mechanism is completely different. There are polar chemical groups on the surface of MA, which make hydrogen bonds with surface -SiOH groups of SiO_2 at RT. After baking at 150 °C the polar groups of MA and -SiOH make covalent bonds. Then strong bonding strength is obtained.

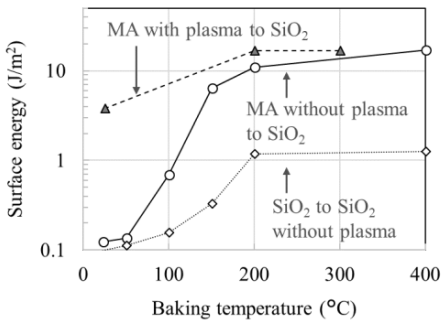

Fig. 2. Surface energy as a function of baking temperature. The connecting lines are guide for the eye.

B. *Chip on wafer with blanket MA film*

Temporary chip bonding at RT by using a blanket MA film was tested. MA-0200 (1 µm thick) was formed after spin-coating a precursor solution of MA onto 4-inch diameter Si wafer and curing for 1 h at 200 °C under N_2. The wafer sample was separated into 10 mm × 10 mm square chips by stealth dicing. The chips were manually picked from the dicing tape and placed on the bonding sample stage. The chips were pre-bonded to a cured MA-0200 coated 4-inch diameter Si wafer at RT under air using a chip placer (FINEPLACER® lambda2, Fintech, Co.). The bonding pressure was 0.2 MPa and it was applied only 1 second. 6 chips were placed on the wafer with a chip-to-chip gap of approximately 0.1 mm. For permanent bonding, the stacked sample was baked at 200 °C for 1 h under N_2 without pressing. As shown in Fig. 3 the 6 chips were pre-bonded at RT. As described in section II. A, MA is spontaneously bondable with point load, so bonding pressure and pressing time can be quite smaller and shorter as well.

C. *Robustness against bonding failure*

The robustness of the MA film against bonding failure due to rigid particles such as Si particles on the bonding interface was investigated. As reported in previous studies [2-3], rigid particles such as Si particles are the main component of large void formation at the bonding interface. The void size parallel to the bonding interface is determined approximately by the height of the rigid particles [2]. In this work, instead of Si particles, Cu pads (10 µm diameter, 430 nm thick, 500 µm pitch) on SiO_2 film on Si substrate (Fig. 4) were used as the rigid material on the bonding interface. After Cu film sputtering, photoresist pattern formation, and wet chemical etching, a uniform Cu pad pattern was formed on the entire surface of a 4-inch diameter Si wafer (525 µm thick). The Cu pad pattern wafer sample was separated to 10 mm × 10 mm square chips by blade dicing. For the removal of surface Si particles, two fluid cleaning was performed. The Cu pad height was measured with a contact type stylus profiler (DektakXT, Bruker. Co.).

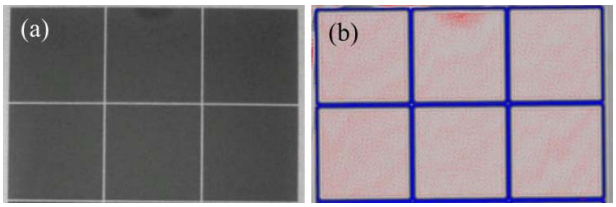

Fig. 3. (a) IR camera image of a chip on wafer stacked sample after pre-bonding at RT. (b) C-SAM image of the same sample after baking at 200 °C under atmospheric pressure.

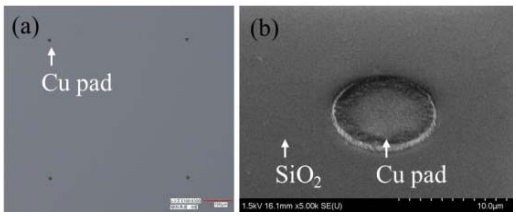

Fig. 4. (a) Optical microscope image of Cu pad (430 nm thick) pattern. (b) SEM image of Cu pad.

MA-0200 film (2.2 µm thick, 200 °C cured) was formed on 4-inch diameter Si wafer, and it was directly placed on the Cu pad patterned chips on the dicing tape under air in clean room condition (class 100). The stacked sample was pressed by a conventional oil press tool at RT. After pressing it for 1min at 1.5 MPa at RT, all Si chips were bonded (Fig. 5(a)). Some of the voids measured are due to visible large particles at the chip edge. After pressing it at 200 °C for 1min the voids decreased and only one small void remained (Fig. 5(b-c)).

The same experiment was also performed for a Cu pad pattern with a thickness of 670 nm. In this case, when the bonding condition is 1.5 MPa at RT, the void area was larger than the result for Cu pad with a thickness of 430 nm. The voids almost disappeared after the pressing at 1.5 MPa at 200 °C (Figure not shown).

For MA-1200, a similar result was obtained with a 430 nm thick Cu pad pattern. On the other hand, many voids were measured in the Cu pad pattern with a thickness of 670 nm (Figures not shown). This is probably due to the high T_g of MA-1200.

For reference, the same bonding test was performed using a Si wafer on which thermally oxidized SiO_2 (200 nm thick) was formed instead of the MA coated wafer. Then the SiO_2 formed Si wafer could not be bonded to the Cu pattern wafer. According to [12], the 0.5 µm height particles make a 0.5 cm diameter void at the bonding interface of two Si wafers with 525 µm thick. Therefore, theoretically, a 430 nm thick Cu pad makes a void with a diameter of 0.43 mm. The diameter is almost equal to the Cu pad pitch (0.5 mm). Therefore, bonding was failed.

From the above results, the two types MAs can be bonded without detectable void by IR or C-SAM even when rigid particles with a thickness of at least 1/5 of the MA film thickness are present on the bonding interface. Since wafer with SiO_2 formed could not be bonded, the smaller elastic modulus of MA compared to SiO_2 is likely the main reason for the undetectable voids. It is presumed that the voids are very small because the MA encapsulates rigid particles by elastic deformation.

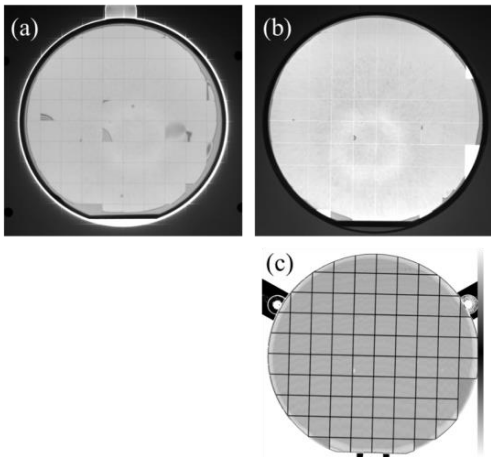

Fig. 5. (a) IR camera image of a stacked sample of Si chips with Cu pads (430 nm thickness) and a Si wafer with MA-0200 (2.2 µm thick) film after pre-bonding at RT with 1.5 MPa. (b) IR camera image of the same sample after bonding at 200 °C with 1.5MPa. (c) C-SAM image of the same sample after bonding at 200 °C with 1.5 MPa.

III. Cu-Cu Hybrid Bonding with MA

A. Test vehicle

Cu-Cu hybrid bonding was performed by using MA-0200. A customized test vehicle (Fig. 6) was fabricated by Waltz Co. based on the original test vehicle (CC40-0101JY and IP40-0101JY). Cu pads with 10 µm diameter, 5 µm thick, and 40 µm pitch were formed as bonding pads on the test vehicle by the semi-additive process. To maintain the global planarity of the bonding layer after CMP, dummy Cu pads were uniformly distributed over the entire area of the test vehicle. The test vehicle has 20 daisy chains with 528 Cu bonding pads in each daisy pattern. The bottom chip has external Cu pads for measuring the resistivity of the connected daisy chain.

B. Hybrid bonding with compression by using MA-0200

A precursor solution of MA-0200 was spin coated onto a test vehicle coupon (3.65 cm × 3.65 cm for top chip and 4 cm × 4 cm for bottom chip) and cured at 200 °C for 1 h under N_2. Then a 4.5 µm thick MA was formed. After CMP using aluminum slurry and colloidal silica slurry, a flat bonding surface consisting of MA and Cu was obtained. The amount of Cu dishing was 10-20 nm. The Ra of Cu was 2.2 nm and the Ra of MA was 0.5 nm.

The two coupons were separated into dies (7.3 mm × 7.3 mm top chip and 10 mm × 10 mm bottom chip) by blade dicing. After two fluid cleaning, chip level CMP was performed to remove Si particles on the Cu surface. Before chip bonding, surface Cu oxides were removed by rinsing with 1 wt% citric acid for 1 min. Then the top and bottom chips were pre-bonded to each other at RT using a chip placer. The stacked chips were pressed at 5 MPa and 400 °C for 30 min using a wafer bonder (EVG501, EVG Co.) for Cu to Cu bonding.

The electrical connectivity of the daisy pattern was measured by the 2-prove method using a manual prober. Then electrical connectivity of daisy chain was measured. Cross sectional SEM measurement of daisy chain were performed. As seen in Fig. 7 there were no voids or no seams at the MA to MA bonding interface.

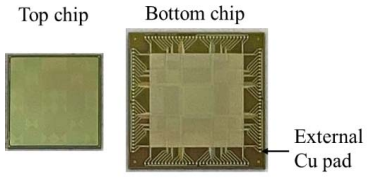

Fig. 6. Optical microscope images of top (left) and paired bottom (right) chips with daisy chains.

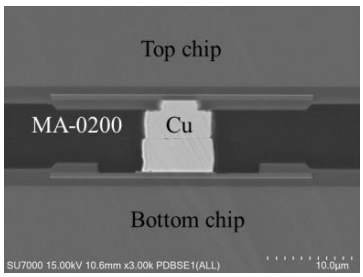

Fig. 7. Cross sectional SEM images of the Cu-Cu hybrid bonding with MA-0200.

If Cu-Cu bonding without pressing is achieved, a batch annealing process become possible, then Cu-Cu bonding throughput is significantly improved. Therefore, hybrid bonding without compression was test by using MA-0200, however, electrical connectivity of daisy chain was not obtained. One of possible reasons of the bonding failure is the thermal expansion of MA at the bonding at 400 °C. Fig. 8 shows the MA thickness from RT to 400 °C. In this measurement, a 20 mm × 20 mm square Si chip with 200 °C cured MA film was placed on a heating stage under N_2 ambient, and the stage temperature was increased from RT to 400 °C without pre-heating. Then the MA film thickness at each temperature was measured using a spectroscopic ellipsometer. The thickness of MA-0200 was always larger than the theoretical thickness of Cu (calculated from the CTE 17 ppm/K). This result indicates that the Cu-Cu gap at the hybrid bonding process increased with increasing temperature. Therefore, it is assumed that Cu to Cu connection was not obtained.

C. Hybrid bonding with compression by using MA-1200

Fig. 8 also plots the thickness of MA-1200. Its thickness was always smaller than that of Cu. This is the result of suppression of thermal expansion due to film shrinkage associated with cross-linking of MA-1200. In this section, prior to the investigation of hybrid bonding without compression, hybrid bonding with compression by using MA-1200 was performed.

The chip bonding procedure of daisy TEG was almost the same to that in section III. B. In this experiment, top chip bonding dielectric was MA-1200 and the bottom chip bonding dielectric was plasma CVD SiO_2. The organic and inorganic asymmetric structure was selected because it offers significant advantages such as relaxation of internal stress during thermal cycle stress (see section V) and improved thermal conductivity (see section VI). CMP of MA-1200 and SiO_2 was performed using a commercially available colloidal silica slurries. The surface SEM images of the bonding layer composed of MA-1200 and Cu were shown in Fig. 9. After optimization of CMP conditions, a quite smooth surface was obtained (Ra 0.1 nm for MA and Ra 0.3 nm for Cu). The dishing amount of Cu was 10-20 nm.

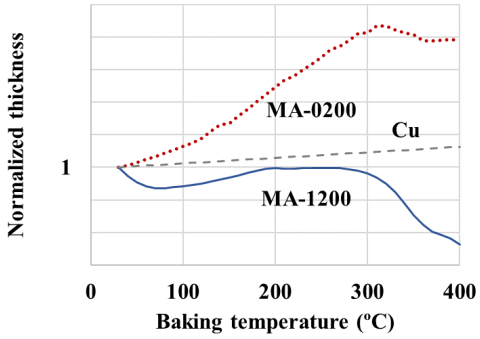

Fig. 8. Measured thickness of MA (200 °C cured) as a function of baking temperature. The Cu data are calculated data.

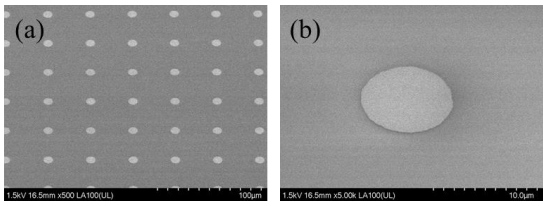

Fig. 9. Bird's eye view SEM images of the bonding layer consisting of Cu and MA-1200 after CMP.

Fig. 10 is C-SAM image of the boded chips (permanent bonding condition was 350 °C for 90 min in N_2 with 5 MPa press). There was no void at the entire bonding interface.

Fig. 11 (a) and (b) are cross sectional SEM images of the bonded chip. From SEM images, there was no seam at the Cu-Cu bonding interface. From the Cu grain boundary map by electron back scattered diffraction pattern (EBSD) analysis, the Cu grains diffused across the Cu-Cu bonding interface, therefore, metallic Cu-Cu bonding was created.

The electrical resistivity of the daisy chain was measured by the 2-prove method. As a result, 100% electrical connectivity was obtained with all 20 daisy chains of 2 bonded samples.

The electrical reliability of the bonded sample was tested by thermal cycling test (JESD22-A104C test condition G: -40 ºC ~ +125 ºC, 2 cycles/hour, 1,000 cycles). Fig. 12 shows the change in resistivity of the daisy chain after 100, 250, 500, 750, and 1,000 cycles relative to the initial value. "Outer chain" is the total resistivity of the 12 daisy chains (including 6,336 Cu to Cu connections) in the outer region of the chip. The "inner chain" is the total resistivity of the 4 daisy chains (including 2,112 Cu to Cu connections) in the center region of the chip. Our criteria of acceptance for change of resistivity is less than ±10%. Both results passed our criteria.

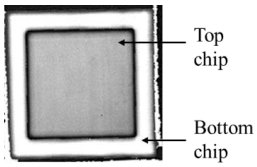

Fig. 10. C-SAM image of the bonded chips where the top chip has a MA-1200 and Cu bonding layer and the bottom chip has a SiO_2 and Cu bonding layer. The bonding condition is 350 ºC for 90 min with 5 MPa press.

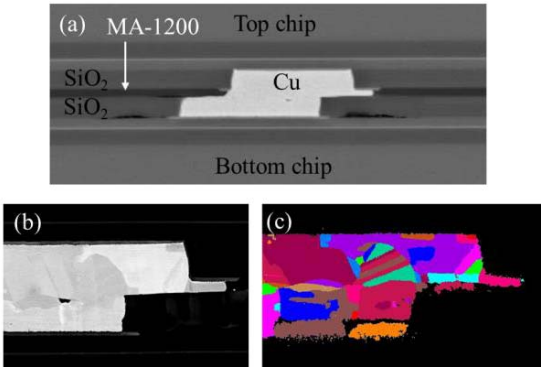

Fig. 11. (a-b) Cross-sectional SEM images of the Cu-Cu hybrid bonding layer. (c) EBSD Cu grain map of the same sample. The bonding condition is 350 °C for 90 min with 5 MPa pressing.

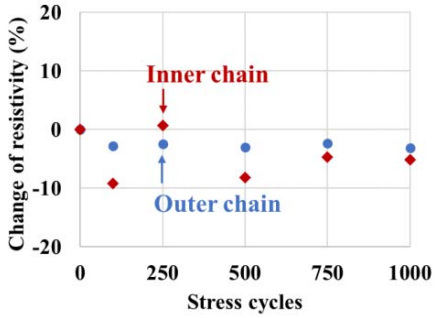

Fig. 12. Change of resistivity of daisy chain relative to the initial value under thermal cycle stress test.

D. Hybrid bonding without compression by using MA-1200

As we mentioned in section III. C, the thickness of MA-1200 is always smaller than that of Cu during the bonding process. It is expected that Cu-Cu bonding with MA-1200 can be achieved without pressing, similar to Cu-Cu bonding with SiO_2 [13-14].

For proof of concept, the same samples of section III. C were pre-bonded by pressing at 0.2 MPa for 1 sec at RT. The bonded sample was baked at 350 ºC for 90 min under atmospheric pressure in N_2. No void was measured by C-SAM (Fig. 13) and Cu to Cu metallic bonding was obtained as shown in Fig. 14.

A thermal cycling test of daisy chains (JESD22-A104C test condition G: -40 ºC ~ +125 ºC, 2 cycles/hour, 1,000 cycles) was performed. Change of the resistivity of the outer and inner daisy chains (Fig. 15) passed the criteria of acceptance (less than ±10%). As a result, as the authors assumed, hybrid bonding without compression was achieved by using the small film shrinkage of MA.

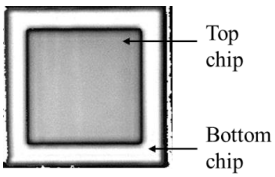

Fig. 13. C-SAM image of the bonded chips where the top chip has a MA-1200 and Cu bonding layer, and the bottom chip has a SiO_2 and Cu bonding layer. The bonding conditions are 350 ºC for 90 min without compression.

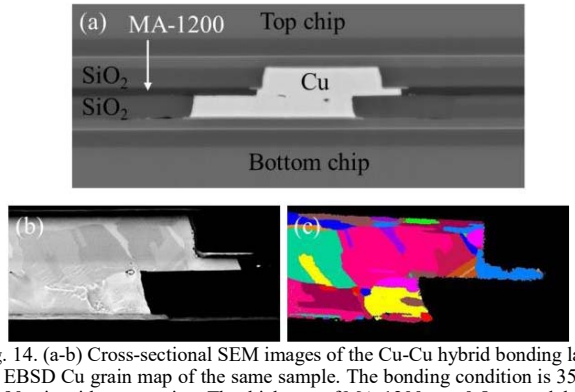

Fig. 14. (a-b) Cross-sectional SEM images of the Cu-Cu hybrid bonding layer. (c) EBSD Cu grain map of the same sample. The bonding condition is 350 ºC for 90 min without pressing. The thickness of MA-1200 was 0.5 µm and the top chip's SiO_2 thickness was 1.5 µm, and the bottom chip's SiO_2 thickness was 2 µm.

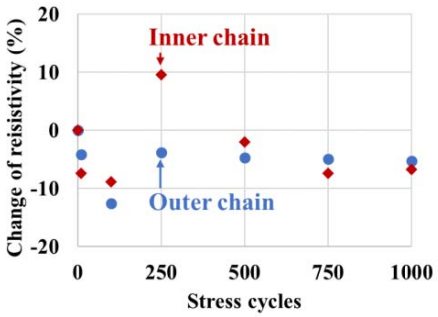

Fig. 15. Change of resistivity of daisy chain under thermal cycle stress test.

E. First trial of fine pitch Cu to Cu bonding

According to more recent work on fine pitch bonding technology, the limitation of solder micro bump is 10-20 µm pitch [1]. In this section, the first trial results for fine pitch (<10 µm) Cu to Cu bonding by using MA is reported.

As a test pattern wafer, a fine pitch Cu pads (3 µm diameter, 6 µm pitch and 0.5 µm thickness) were fabricated. In the fabrication, a Cu film was sputtered on a SiN film on a 8 inch diameter Si wafer, a photoresist was formed on it, wet chemical etching was performed, and then the Cu pad pattern was obtained. A precursor solution of MA-0200 was spin coated on it and cured at 150 ºC for 1h. The target thickness of MA-0200 was 1 µm. A flat bonding surface obtained after CMP with colloidal silica slurry. Cu dishing amount was 10-15 nm. Fig. 16 show SEM images of the surface of the bonding layer consisting of MA and Cu pads. There was no obvious contamination of MA on the Cu surface and no Cu contamination on the MA surface.

Wafer sample was separated into 10 mm × 10 mm chips by blade dicing. The chip surface was polished by chip level CMP to remove Si particles on Cu pads, and rinsed with CMP-B01 (Kanto Chemicals, Inc.). Two chips were pre-bonded to each other using a chip placer (Fintech Co. Chip Placer) under clean room conditions with 0.2 MPa press at RT for 1 sec. The stacked chips were baked at 200 ºC for 1h under N_2 without pressing to achieve permanent bonding of MA to MA and Cu to Cu simultaneously.

Fig. 17 shows cross sectional SEM images of the bonded chip. No seams were measured at the MA-MA bonding interface. There was no gap at the Cu to Cu bonding interface, but seams were clearly observed. Therefore Cu grain growth across the bonding interface was not achieved with MA-0200 under this bonding condition. Results by using the MA-1200 will be reported in our future articles.

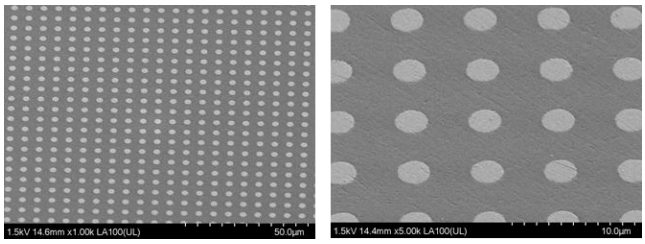

Fig. 16. Bird's eye view SEM images of the bonding layer consisting of MA-0200 and Cu pads after CMP.

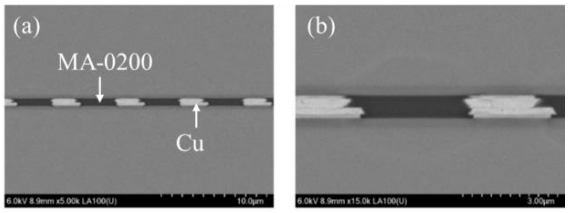

Fig. 17. Cross sectional SEM images of a bonded chip having a bonding layer composed of MA-0200 and Cu. The bonding conditions were 200 ºC for 1 h without pressing.

IV. CU ION MIGRATION TORELANCE

From a reliability perspective, the Cu ion migration tolerance of the bonding dielectrics is the most important factor to prevent electrical shorts across bonding dielectrics. In our proposed Cu hybrid bonding process (Fig. 1), MA is directly coated on Cu pads without barrier metal. Therefore, the MA's Cu ion migration tolerance was examined under harsh test conditions.

For the examination of Cu ion migration tolerance of MA-1200, MA-1200 was formed on a Cu comb pattern with 2.5 mm length and 5 µm width Cu lines, and 5 µm width spaces. Curing conditions for MA-1200 were 350 ºC for 1 h. Fig. 18 shows the resistivity of MA-1200 on Cu comb pattern under 130 ºC, RH 85%. The bias voltage for the Cu pattern is 9.25 V. After 96 h, the resistivity was kept the same order to the initial resistivity. Fig. 19 are the optical microscopic images of the samples before and after biasing. There was no Cu migration such as Cu dendrite growth.

As another Cu ion migration test, MA-1200 coated Cu comb pattern was baked at 400 ºC for 1h under N_2 ambient. Fig. 20 (a) is a cross sectional SEM image of the baked sample and Fig. 20 (b) is a Cu map by energy dispersive X-ray spectroscopy (EDX). There was no Cu ion migration from Cu to MA-1200. In addition, there were no failures such as voids and delamination of MA-1200. Therefore, it is concluded that MA-1200 has good Cu ion migration tolerance even after high temperature process of Cu to Cu bonding.

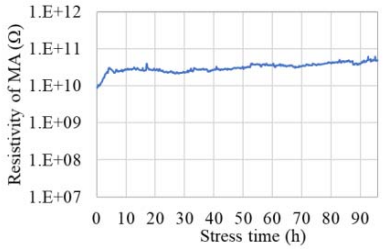

Fig. 18. Electrical resistivity of MA-1200 on Cu comb pattern with 5 µm lines ad 5 µm spaces, under biased HAST (130 ºC, RH 85%, 9.25 V).

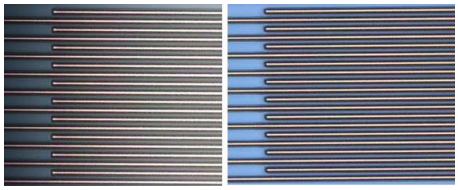

Fig. 19. Optical microscopic images of MA-1200 on the Cu comb shaped pattern of the sample before (left) and after biased HAST (right).

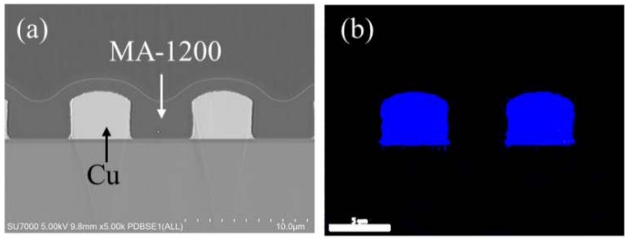

Fig. 20. (a) Cross sectional SEM image and (b) EDX Cu map of MA-1200 on Cu comb pattern after baking at 400 ºC for 1h under N_2.

V. INTERNAL STRESS SIMULATION

A CTE mismatch between the bonding dielectrics and the bonding Cu pad is possible to cause some mechanical failures such as delamination and cracking under thermal stress conditions. These failures result in electrical failures. Numerical calculations on internal stress were performed for a theoretical explanation of the good thermal cycle stress test results reported in section III.

Fig. 21 shows a numerical simulation model for calculation of the internal stress at the bonding layer. The Cu pad diameter is 10 µm, the Cu pad pitch is 40 µm, and the total Cu pad thickness is 4 µm. It was assumed that the internal stress is zero at 23 ºC. Tthe internal stress at +150 ºC and -50 ºC was calculated.

In this calculation, the authors focused on the internal stress of the Cu bonding pad in the z-direction (perpendicular to the bonding interface). The most probable failure mode under thermal stress could be delamination at bonding interface of Cu, as it could be due to the CTE mismatch between MA, SiO_2 and Cu. Fig. 22 shows the internal stress map of the cross-sectional area around the bonding layer. In the case of SiO_2 to SiO_2 direct bonding (Figs. 22(a) and (b)), strong plus stress was measured at +150 ºC. This is because the thermal expansion of Cu is larger than that of SiO_2. At -50 ºC minus stress was measured. This is because the thermal shrinkage of Cu is larger than that of SiO_2. On the other hand, when the bonding layer consists of SiO_2 and a thin MA-1200 layer (500 nm thick), small plus and minus stresses were measured at +150 ºC and -50 ºC, respectively.

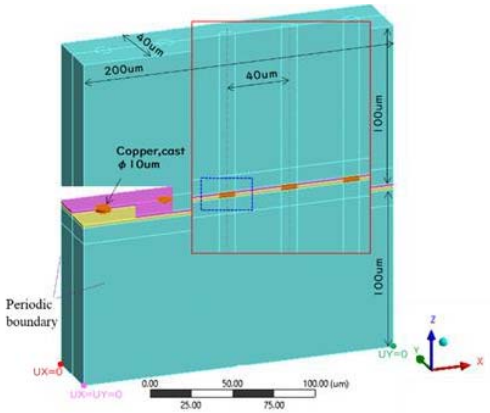

Fig. 21. Numerical simulation model for internal stress in bonding layer.

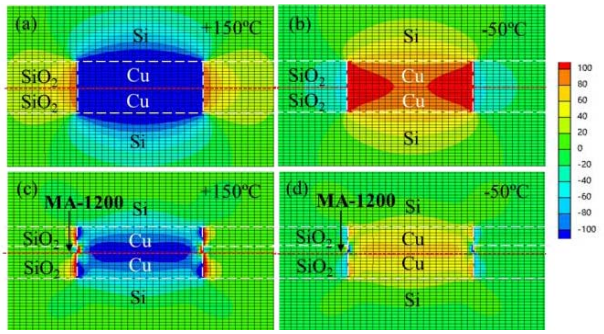

Fig. 22. Internal stress map in z-direction. (a) Stress map at 150 ºC for a bonding layer consisting of two SiO_2 (2 µm thick) layers. (b) Stress map at -50 ºC for a two SiO_2. (c) Stress map at 150 ºC for a SiO_2(1.5 µm)/MA-1200(0.5 µm)/SiO_2(2 µm). (d) Stress map at -50 ºC for a SiO_2(1.5 µm)/MA-1200(0.5 µm)/SiO_2(2 µm).

Fig. 23 plots the stress in z-axis at the Cu-Cu bonding interface as a function of the x-coordinate. In the case of SiO_2 to SiO_2 direct bonding, large plus stress (100-120 MPa) was measured in Cu at -50 ºC. On the other hand, in the case of SiO_2 with a thin MA-1200 layer, the stress in Cu at -50 ºC reduced (65 MPa). The reason for the reduction of internal stress in Cu by the MA-1200 thin layer is the mitigation of the shrinkage stress of Cu against SiO_2 by the expansion stress of MA-1200.

From above results, it is concluded that the internal stress of the bonding layer with thin MA-1200 layer is smaller than that of SiO_2 direct bonding.

VI. THERMAL CONDUCTIVITY SIMULATION

The thermal conductivity of bonding layer containing adhesive is one of the main concerns for heat sensitive devices such as DRAM, since the thermal conductivity of adhesive is always lower than that of inorganic dielectrics. Thermal conductivity of the bonding layer was numerically calculated by using ANSYS POLYFLOW. The numerical calculation model is shown in Fig. 24. It is assumed that a bonding layer consisting of dielectric 1 and Cu pads and the another bonding layer consisting of dielectric 2 and Cu pads were bonded. Each thickness of dielectric 1 and dielectric 2 was 2 µm. The Cu diameter and Cu pitch were 10 µm and 40 µm or 5 µm and 10 µm. In this calculation, thermal conductivity of Cu is 390 W/(m K), that of SiO_2 is 1.0 W/(m K), and that of MA is 0.25 W/(m K).

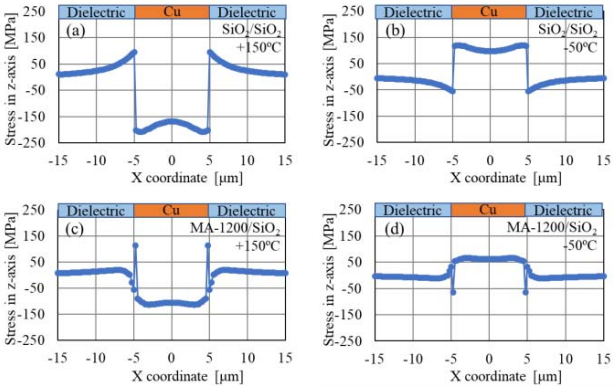

Fig. 23. Internal stresses in the z-direction whose data extraction lines are plotted as red dotted line in Fig. 22. The extraction lines exist at the Cu-Cu bonding interface.

TABLE II summarized the calculation results. For both Cu 40 µm and 10 µm pitches, the thermal conductivity in the z-direction (perpendicular to the bonding interface) weakly depends on the MA occupancy. On the other hand, the thermal conductivity in the x-direction (horizontal to the bonding interface) strongly depends on the MA occupancy. In the actual device, thermal conductivity in the z-direction is most important because generated heat in the ICs escape via Cu through silicon via and heatsink. In addition, it is worth noting that the thermal conductivity in the z-direction is strongly improved in fine pitch Cu (5 µm diameter and 10 µm pitch). This result inspires us to place fine pitch dummy Cu pads uniformly on entire area in the bonding layer for thermal conductivity improvement.

VII. CONCLUSION

A new adhesive (MA) was developed for high throughput and low temperature chip on wafer hybrid bonding. Chip on wafer bonding test by using MA with Cu pads showed that MA is pre-bondable at RT with 0.2 MPa and 1 second chip compression. In addition, by using the slight film shrinkage of MA at the Cu-Cu bonding process at 350 ºC for 90 min, Cu-Cu connectivity without compression was demonstrated. Therefore high throughput processes such as chip pre-bonding at RT of a large number of chips on a wafer and batch annealing process for Cu-Cu bonding can be realized by using MA.

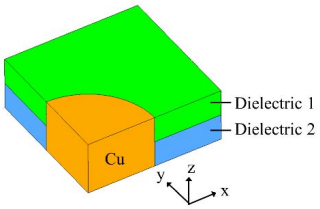

Fig. 24. An image of numerical simulation model for thermal conductivity. Each thickness of the dielectric 1 and dielectric 2 was fixed to 2 µm, respectively.

TABLE II. CALCULATED THERMAL CONDUCTIVIYT IN Z AND X DIRECTION

Cu diameter/pitch	Dielectric 1	Dielectric 2	z-direction W/(m K)	x-direction W/(m K)
10 µm/40 µm	SiO_2	SiO_2	20.1	1.10
10 µm/40 µm	MA	SiO_2	19.7	0.69
10 µm/40 µm	MA	MA	19.4	0.28
5 µm/10 µm	SiO_2	SiO_2	77.3	1.49
5 µm/10 µm	MA	SiO_2	77.0	0.93
5 µm/10 µm	MA	MA	76.7	0.37

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