Scalable Fiber-Array-to-Chip Interconnections with Sub-Micron Alignment Accuracy

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Abstract— Experimental demonstration of optical fiber array-to-chip assembly is realized with a passive self-alignment mechanism and 3D-printed ferrules. The approach explored in this paper allows an array of fibers to be interconnected to chip-level grating couplers (GCs) with sub-micron level placement accuracy. The mechanical alignment (verified to be stable over one year) enables high relative coupling efficiency (>75%) at 1550 nm. It is shown that the proposed fiber interconnection technology is compatible with 2.5D heterogeneous integration technologies.

Keywords—optical interconnects, packaging, self-alignment, surface coupling

I. INTRODUCTION

The exponential growth of internet traffic is placing great pressure on the infrastructure of the data-communication industry requiring very high-bandwidth modules with extreme energy efficiency [1, 2]. These requirements drive the need for co-packaged optics (CPO) for several reasons. First, the bandwidth capacity of optical fibers is much larger than that of electrical interconnects at the board/package level [3]. Second, optical-to-electrical interfaces are placed much closer to the computing chip in CPO thereby reducing the length and parasitics of the electrical interconnects, which result in improved signal integrity and energy efficiency [4]. Third, with increasing level of integration and compatibility with mature semiconductor technologies (e.g., complementary metal oxide semiconductor (CMOS) process and flip-chip bonding equipment), there are cost benefits for CPO [5, 6].

One critical component of CPO design is the coupling between the fiber and the chip. Major options for the interfaces are as follows: 1) edge coupling; 2) surface coupling and 3) free-form optics. The performance of these approaches is compared in Table I [7-11]. Edge coupling features typically low-coupling loss (<1 dB) with relatively wide bandwidth (>100 nm) as well as insensitivity to polarization [7, 8]. However, this method also faces some limitations including 1) tight alignment tolerance, 2) large footprint, 3) special fiber tips in some demonstrations, and 4) incompatibility with wafer-level test. The surface coupling method, however, provides 1) area-array fiber-coupling (larger bandwidth density) with compact couplers, 2) flexibility in placement and routing of devices and 3) access to the whole surface area. It should be noted that low coupling loss using gratings has been recently shown experimentally (0.8 dB with 47 nm spectral bandwidth for 1-dB window) [9]. The free-form optics has been used to perform impressive demonstrations but is limited in adoption at this stage [11].

In the present work, a fiber-to-chip optical interconnection technology called fiber interconnect silicon chiplet technology (FISCT) is shown to be scalable and compatible with 2.5D heterogeneous integration technologies. This paper extends prior work on FISCT [12]. The envisioned co-packaged photonics 2.5D platform using FISCT is shown in Fig. 1 where photonic connectivity is placed directly adjacent to a group of logic and memory chiplets, which are all located on a common interposer with high-bandwidth electrical interconnects. The key features of FISCT are 1) the passive self-alignment of the
optical fibers to the underlying photonic integrated circuit (PIC),
2) a chiplet based solution for fiber alignment and interconnection, 3) the use of 3D printing to enable precise array-area optical fiber ferrules that are integrated within a silicon chiplet.

This paper is organized as follows: Section II describes the design of FISCT and the layout of the PIC. Fabrication and assembly of FISCT are described in Section III. Section IV reports the optical test setup and results. The conclusion is presented in Section V.

II. DESIGN OF THE INTERCONNECTS

A schematic of the FISCT platform is illustrated in Fig. 2. FISCT is comprised of three components: 1) fiber-insertion ferrules, 2) fiber-carrier die, and 3) PIC (substrate) with grating couplers and ridge waveguides. Three mechanical interfaces are designed to ensure precise placement of the components: a) matching of positive self-alignment structures (PSAS) and inverse pyramid pits on a silicon carrier; b) 3D printed fiber ferrules integrated within the silicon carrier; c) insertion of SMF-28 optical fibers into the holes formed in the 3D printed fiber ferrule.

In this work, four FISCT bonds are formed on a 30 mm by 30 mm PIC substrate. Each FISCT carrier die is 8 mm by 8 mm. Further, each carrier die accepts four 3D printed ferrules with each containing ten fiber-insertion holes. A layout of the PIC under one carrier die is shown in Fig. 3. FISCT-to-PIC self-aligning structures are placed at the four corners of the carrier die (blue squares in Fig. 3); reflowed photoresist domes are used on the surface of the PIC and anisotropic-etched inverse pyramid pits are formed on the bottom of the carrier die.

To quantify the alignment of carrier dice to the substrate, four sets vernier marks (red and teal stripes in Fig. 3) are placed on the four edges of each carrier die. Each set of marks has three levels measuring placement accuracy at 2 μm, 1 μm, and 0.5 μm, respectively. The optical coupling performance is evaluated by grating couplers connected by straight ridge waveguides with two different lengths of approximately 280 μm and 710 μm (golden lines in Fig. 3). The focusing grating coupler occupies a footprint of approximately 15 μm x 25 μm.

III. FABRICATION OF COMPONENTS

A. Fabrication of PIC

The passive PIC is fabricated on SOI wafer with a device layer of 220 nm thickness and a buried oxide (BOX) thickness of 3 μm using e-beam lithography (EBL). Following resist patterning, the device layer is then dry-etched in inductively coupled plasma etcher with Cl₂.

B. Fabrication of Carrier Dice

The carrier dice are fabricated at the wafer level (Fig. 4). The starting wafer is a 300-μm thick double side polished (DSP) Si wafer with (100) orientation. The wafers are first thoroughly cleaned with piranha solution (H₂SO₄: H₂O₂ at 5:1). The wafers are then coated with low-stress silicon nitride in a low-pressure chemical vapor deposition (LPCVD) furnace. The resulting thickness of the SiN is approximately 200 nm. Patterning of the vernier marks is done by partial etching of the nitride layer with details described in Subsection E. Photolithography by mask-less aligner (MLA) at a resolution of 0.5 μm is performed to pattern 1) the through anisotropic-etched inverse pyramid pits for 3D printed ferrule insertion and 2) the alignment pits that are precisely matched to the re-flowed domes (located on the PIC). The nitride film in those regions is then etched away using reactive ion etching. Next, the wafer is then immersed into a KOH solution at 90 °C to form the inverse pyramid pits that are on the carrier.

The wafer is then diced into carrier dice and cleaned in an acetone bath. After removal of the nitride layer on the other end of the through anisotropic-etched inverse pyramid pits, the 3D-printed ferrules are inserted into the carrier dice and latched with segments of 250 μm-thick optical fiber (for demonstration purposes).

C. Fabrication of Positive Self-Alignment Structures

Self-alignment using PSAS has been previously developed and demonstrated extreme alignment accuracy [13]. This work
leverages the previously developed self-alignment technology for FISCT with optimized process conditions.

D. Fabrication of Fiber Ferrules

The fiber ferrules are fabricated by 3D-printing via two-photon lithography process. This fabrication method enables fine-tuning of 3D features at sub-micron scale. Further, the 3D printing process can naturally be leveraged to compensate for any systematic fabrication errors in FISCT. With careful design and measurement, such variations or errors due to our cleanroom setting are quantified in terms of their impact to the alignment interfaces. The output of this is then used to adjust the 3D-printed fiber ferrule prior to its integration into the carrier dice. Specifically, the x-y axis placement of the fiber insertion holes as well as the width and length of the ferrule sidewalls are adjusted (Fig. 5) at the sub-micron scale to compensate for systematic errors encountered in our cleanroom.

As shown in Fig. 5, other important features in the ferrules are a) funnel-shaped opening designed to guide fiber-insertion and b) four inner ridges along the through holes to confine the fibers.

E. Fabrication of Vernier Marks

Vernier marks are placed on the four edges of each die (Fig. 3). As for the carrier dice, the marks on the nitride layer are patterned by EBL before the patterning of other features including the ferrule-insertion holes and dome-matching pits. The pattern is then partially etched into the nitride layer with a remaining thickness of 120 nm, which is enough to protect the Si substrate in those regions from the subsequent wet-etching step while maintaining enough contrast for measurement. The alignment marks on the SOI, however, are fabricated together with the PIC in the device layer (using the the same lithography step). The difference in the light transmittance (wavelength around 1.1 μm) between the Si and the surrounding oxide is also significant enough to form clear contrast in infrared microscopic images during the alignment measurements.

F. Assembly of FISCT and Alignment Measurement

Once all components are fabricated, the 3D-printed ferrules are inserted into the carrier dice. An array of 2X2 FISCT assemblies is shown in Fig. 6, where the carrier dice are secured on the PIC using epoxy. Within each carrier die, four through inverse-pyramid through holes are available, each containing 10 fiber-insertion holes (in the 3D printed fiber-ferrule).

The assembly of the carrier dice with ferrules is done manually under a stereomicroscope due to the large tolerance to initial misalignment. This can also be achieved with a pick-and-place tool that has relatively poor alignment as the fabricated self-alignment features can easily compensate for large initial misalignments.
Typical microscopic images of the alignment results are shown in Fig. 7. Most of the marks have the center lines matched indicating an alignment within 0.5 μm. Table II shows the alignment on the four edges of all four carrier dice on the PIC is controlled within ±1 micron. Such sub-micron accuracy is maintained over one-year, demonstrating the successful design, fabrication, and assembly of FISCT.

IV. OPTICAL TEST RESULTS

The optical test configuration is shown in the block diagram of Fig. 8. The laser outputs a 2.5 dBm continuous wave at 1550 nm. The polarization controller is set to maintain the transverse electric (TE) polarization (parallel to photonic chip surface) at the end of the optical fiber. The optical intensity is collected by an optical spectrum analyzer and an optical power meter, which are both connected to a computer for data acquisition and processing.

Before the optical loss of the assembled FISCT is measured, a benchmark test is performed device-by-device (grating coupler) with the same overall measurement configuration using an active alignment stage with 3-axes positioning accuracy within 0.25 μm (lower right section of Fig. 8).

As a benchmark, the output signal intensity of the grating coupler devices was first characterized with intentional offsets in all X, Y, and Z axis from the optimum location. The 3-dB loss of the optical intensity corresponds to approximately ± 2.5 μm of misalignment in either the X- or Y-direction, while an offset of ± 7 μm in either the X- or Y-direction results in a 10-dB loss relative to that of the optimum location. The performance from device-to-device is consistent for the grating couplers fabricated in the same batch. The systematic deviation value of the benchmark measurement is approximately ± 0.1 dB. Furthermore, the polarization-dependent loss (PDL) of the grating couplers is determined to be around 11.5 dB between TE and transverse magnetic (TM) mode.

Because of the precise alignment of the carrier die to the PIC and the accurate 3D printing, the alignment of the fibers to the grating couplers are controlled at the sub-micron level. This is supported by optical testing with the assembled FISCT, which demonstrates a low coupling loss of 0.1 dB (79%) relative to that of the optimal result from the active alignment benchmark. Because the coupling efficiency is greatly affected by alignment accuracy at the submicron level, we investigated this relationship further by manually introducing intentional offsets into the positions of the grating location relative to the optical fiber and then determining the correlation between the coupling loss and the misalignment value. With the misalignment value increasing from half a micron to nearly one micron, the optical loss increases gradually from 0.1 dB to 0.5 dB. This trend is consistent with the data recorded in the active alignment benchmark.

V. CONCLUSION

In summary, this work has demonstrated a fiber-array to chip optical interconnect using surface coupling method compatible with 2.5D heterogeneous integration. The unique design and fabrication of the mechanical interfaces utilizing lithography and 3-D printing methods have enabled sub-micron level accuracy across carrier dice with long-term stability. The coupling efficiency of this self-alignment assembly is comparable to that of active alignment (79%) making it a promising solution for fiber-to-chip interconnection.

REFERENCES


