2.5D MCM (Multi-chip Module) Technology Development for Advanced Package

Laurene Yip
MediaTek Inc
San Jose, CA, USA
laurene.yip@mediatek.com

James Tsai
MediaTek Inc
Hsinchu, Taiwan
james-yl.tsai@mediatek.com

Rosa Lin
MediaTek Inc
Hsinchu, Taiwan
rosa.lin@mediatek.com

Ian Hsu
MediaTek Inc
Hsinchu, Taiwan
ian.hsu@mediatek.com

***Abstract*—2.5D silicon interposer packages have been widely adopted for high-end applications such as datacenter, networking, and artificial intelligence. To meet the increasing demand for higher performance and greater bandwidth, the die and package sizes have been increasing due to the need for higher levels of device integration. As the package size increases, chip-to-package interaction (CPI) will become more challenging to manage. The main challenges with large 2.5 devices are warpage, C4 bump integrity, underfill cracking, and mold compound delamination caused by interposer corner stress. In our study, package warpage and reliability of a chip-on-wafer-on-substrate (CoWoS) multi-chip module (MCM) package with two 1.5X reticle interposers and a package size of 85mmX85 mm were investigated. The coefficient of thermal expansion (CTE) mismatch between different package materials can cause warpage and induce mechanical stresses that can lead to bump cracks, underfill delamination/cracking, and other failures in the package. We will discuss package design methods to reduce interposer die stress to enhance package reliability. By using finite element stress analysis to optimize the device layout, C4 bump standoff height, and interposer structure, large size 2.5D MCM packages were developed and evaluated with reliability testing.**

Keywords—2.5D, Multi-chip Module, interposer, package warpage, CoWoS, reliability

I. INTRODUCTION

The growing demands in high performance computing and artificial intelligence are fueling the development of advanced packaging solutions for high performance devices. 2.5D packages with through-silicon via (TSV) interposers have emerged as an attractive packaging solution for heterogenous integration. CoWoS technology enables high levels of integration, improved electrical performance, and high transmission rates. By using TSV interposers to integrate the system-on-chip (SoC) and high bandwidth memory (HBM), system performance can significantly improve because the memory is moved much closer to the logic die resulting in shorter time delays and lower energy consumption.

As device complexity and package size continue to increase to accommodate the integration of more dies, reliability challenges arise. As the die size increases, the package stress also increases due to the CTE mismatch between the die and the substrate, which increases the risk for package failures caused by bump cracks, underfill delamination, and mold compound cracks.

Our study discussed the development of a CoWoS package assembled with two 1.5X interposers. Each interposer integrated a SOC die with multiple HBMs. Warpage and reliability are affected by the package materials, process, and chip module structure design. This paper focuses on optimizing the interposer module design based on simulation and test vehicle results. The package robustness was investigated using component-level reliability testing, which included temperature cycling (TC), an unbiased highly accelerated temperature stress test (uHAST), and a high-temperature storage (HTS) test.

II. PACKAGE DESCRIPTION

In our study, the multi-chip CoWoS packages made with two 1.5X reticle size interposers were evaluated. The SOC and HBMs were connected to the interposer using 40um pitch micro-bumps. The interposer module was assembled onto an 85mm X 85mm organic substrate with 150 um pitch copper pillar C4 bumps. The cross section of the package is shown in Figure 1. Underfill1 (UF1) filled the gap between the die and the interposer while underfill2 (UF2) filled the gap between the interposer and the substrate. Epoxy mold compound was used between the SOC and memory dies to provide structural stability. The package had a copper stiffener ring for warpage control. The assembled package is shown in Figure 2. The key attributes of the test vehicles are summarized in Table 1.

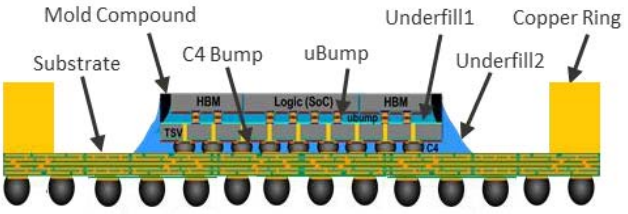


Figure 1. Cross section of the CoWoS MCM package

2377-5726/23/$31.00 ©2023 IEEE
DOI 10.1109/ECTC51909.2023.00135

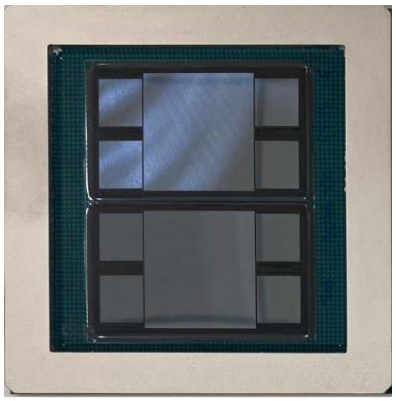
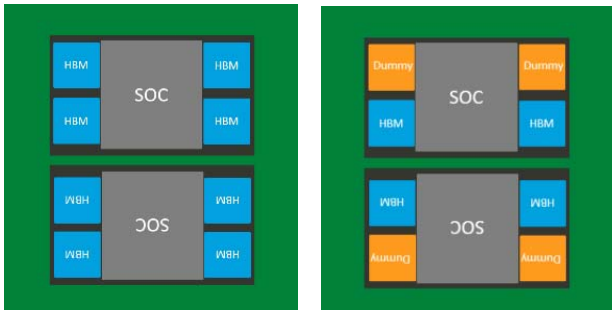


Figure 2. CoWoS MCM device

TABLE I. PACKAGE ATTRIBUTES

Attribute	Item	Dimension
Chip	SoC size (mm2)	27 x 18
	HBM2E size (mm2)	11 x 10
Silicon Interposer	Size (mm2)	1.5 reticle
Organic substrate	Size (mm2)	85 X85
	C4 bump Pitch (um)	150
	BGA Pitch (mm)	l.0

Our study evaluated two interposer configurations. TV1 consisted of 2 interposer modules with a SOC and 4 HBMs integrated on each interposer while TV2 had 2 interposers with 2 HBMs and 2 dummy filler dies on each interposer as shown in Figure 3.



TV1 **TV2**

Figure 3. Interposer floor plans

III. RESULTS AND DISCUSSION

A. Package Warpage Assessment

Warpage of the assembled package affects the device manufacturability and assembly yield. Package warpage is caused by the CTE mismatch between silicon and the package materials and is highly dependent on the interposer module layout design. Since epoxy mold compound (MC) surrounds the dies on the interposer in the 2.5D package, it is important to have a suitable floor plan to avoid large areas of mold compound. An unbalanced structure increases internal package stress, which increases the risk for C4 bump non-wetting or bridge bump, or underfill delamination or cracks. Therefore, the chip module structure can be more balance by incorporating dummy filler dies than without the filler dies.

The package warpage behavior for TV1 and TV2 are shown in Figure 4. Both packages were convex warpage shape at room temperature but turned to a concave shape at 250°C. TV2 with dummy filler die at the interposer corners had higher warpage than TV1 which were populated with HBMs only. At room temperature, the warpage for TV2 was 27% larger than for TV1. At 250C, the warpage for TV2 was 13% higher than for TV1. The lower warpage of TV1 is primarily resulted from a more balance structure with 4 HBMs vs 2 HBMs and 2 dummy dies.

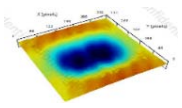
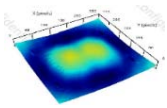
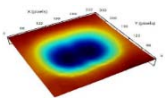
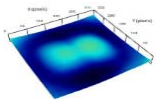
		Room Temp (25°C)	**High Temp (250°C)**
Warpage	TV1		
 (-) Convex		-198 um	153 um
	TV2		
 (+) Concave		-250 um	173 um

Figure 4. Package warpage contour plots (BGA side is up)

Our study showed that having 4 HBMs provide a more balanced structure than using dummy filler die. The warpage difference is attributed to the construction difference between the HBM and the dummy die. A HBM module consists of a base die at the bottom and multiple core DRAM dies vertically stacked and connected with TSVs and micro-bumps on top of the base die. The DRAM die surroundings are encapsulated with epoxy mold compound material for the side mold. The difference in construction between the HBM and dummy die affects the warpage behavior of the module.

B. Package Relability Assessment

During the package development stage, both TV1 and TV2 were subjected to thermal cycling testing to check the package robustness. After TCG 200 cycles, TV1 passed but TV2 failed due to cracks in underfill2 between the interposer and substrate. The underfill cracks were located at the interposer die corner as shown in Figure 5. Underfill cracking can also lead to substrate cracking as shown in Figure 6.

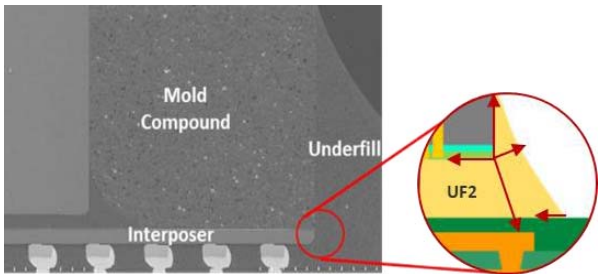


Figure 5. Stress concentration point at interposer corner

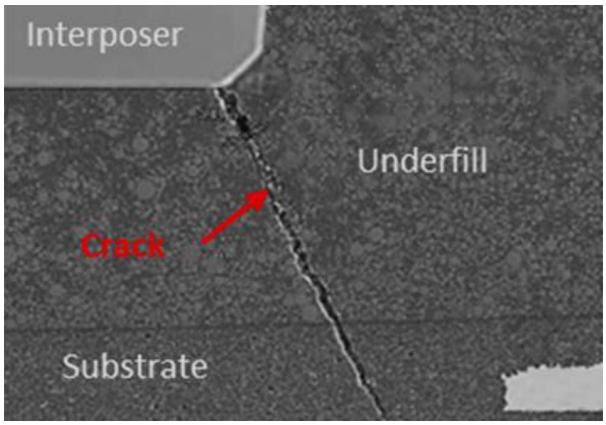


Figure 6. Underfill crack at interpser corner of TV2

Units with a low C4 bump height had a greater risk for underfill cracking. Cross section of failed units showed that underfill cracking were primarily found in units with low bump height. Figure 7a shows a failing unit with low bump height that resulted in underfill cracking at the corner of the interposer while Figure 7b shows a passing unit that had a standard bump height and no underfill cracking.

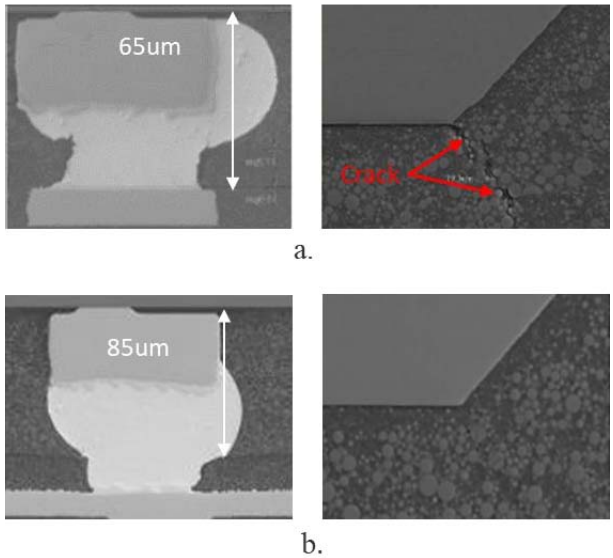


Figure 7. a) C4 bump with low bump height causing underfill crack
b) Standard C4 bump height with no underfill cracking

C. *Package Design on Reliabliity*

Since package warpage and die corner stress are key metrics for component reliability, finite element analysis (FEA) was conducted to analyze the effect of the interposer layout design, interposer thickness, and C4 bump height on interposer corner stress. By reducing the interposer corner stress, the underfill crack risk can be lowered.

D. *Floorplan Design*

The FEA results comparing the corner stress from the floorplans TV1 and TV2 are shown in Figure 8. The simulation data showed the TV2 floorplan with the dummy die at the interposer corners had 4% higher corner stress than TV1. The higher corners stress was attributed to the dummy silicon die having a higher CTE mismatch to the substrate than the effective CTE of the HBM module which is comprised of a higher CTE material set with the underfill and HBM side mold.

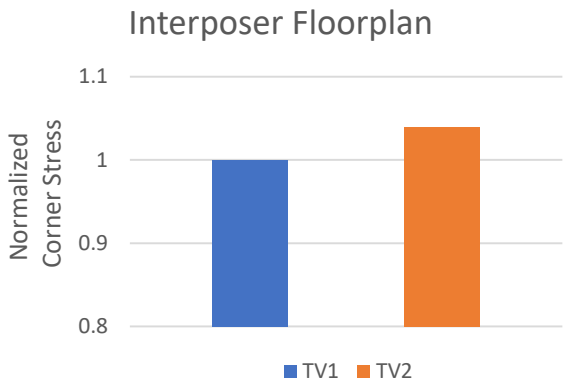


Figure 8. Effect interposer floorplan on interposer corner stress

E. *Interposer Thickness Effect*

Simulation results showed that a thinner interposer could reduce interposer corner stress as shown in Figure 9. By decreasing the interposer thickness from 100 um to 50 um, a 20% reduction in corner stress can be achieved for both test vehicles. The CTE of the silicon interposer is ~4 ppm/K, which is smaller than the underfill2 CTE (~20ppm/K) and substrate CTE (~15 ppm/K). Thus, a reduction to the interposer thickness from 100 um to 50 um effectively reduces the CTE mismatch effect during thermal cycling. The underfill crack risk could be minimized with smaller package deformation, especially at the package corner, during thermal cycling.

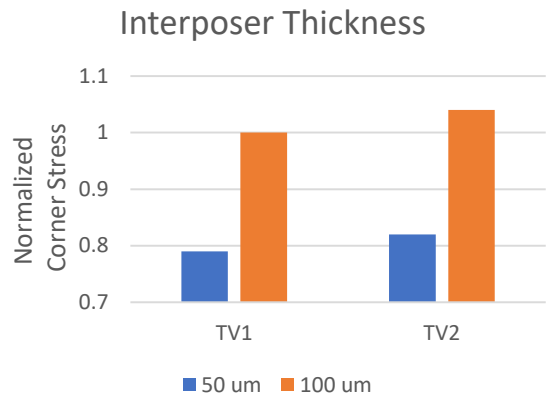


Figure 9. Effect of interposer thickness on interposer corner stress

F. *Bump Height Effect*

The C4 bump height also affects interposer corner stress. From the simulation results, a lower standoff increases interposer corner stress as shown in Figure 10. For TV2, decreasing the standoff from 90um to 60um increases interposer corner stress by 16%. Lowering the C4 bump standoff reduces the underfill amount between the interposer and substrate and increases the underfill fillet height at interposer edge/corner, which induces more corner stress. As a result, C4 bump standoff height control is critical to large-size package reliability.

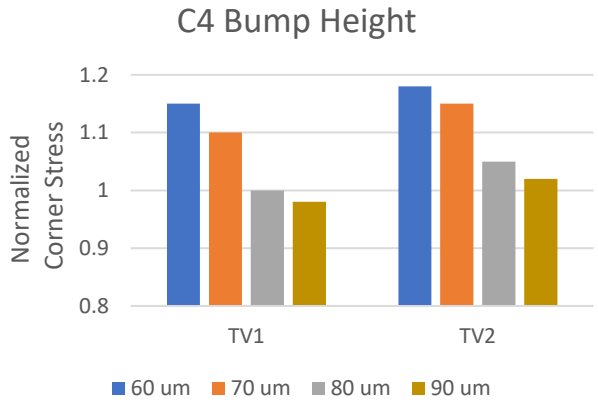


Figure 10. Effect of C4 bump height on interposer corner stress

G. *Reliability Performance*

After optimizing the package structures, the CoWoS MCM packages were subjected to the standard JEDEC reliability tests including moisture soaking level 4 (MSL4) as preconditioning, temperature cycling test (TCT) with -40°C to 125°C (condition G), unbiased high accelerated stress test (UHAST) with 110°C/85%RH, and high temperature storage test (HTS) at 150°C. After reducing the interposer thickness and increasing the C4 bump height, TV2 passed the reliability tests without any failures as shown in Table II. After reliability testing, extensive failure analysis was performed to check the integrity of the C4 joints and underfill. Cross-sectional analysis of the units showed no bump cracks or delamination/cracks in the underfill1 (UF1) between the die and interposer or underfill2 (UF2) between the interposer and the substrate as shown in Figures 11-14.

TABLE II. 2.5D MCM RELIABILITY TEST RESULTS

Test Conditions	TV1	TV2	
Interposer Thickness	100 um	100 um	50 um
MSL4	Pass	Pass	Pass
uHAST 264 hrs (110°C/85%RH)	Pass	Pass	Pass
TCG 1000 cycles (-40 to 125°C)	Pass	Fail	Pass
HTS 1000 hrs (150°C)	Pass	Pass	Pass

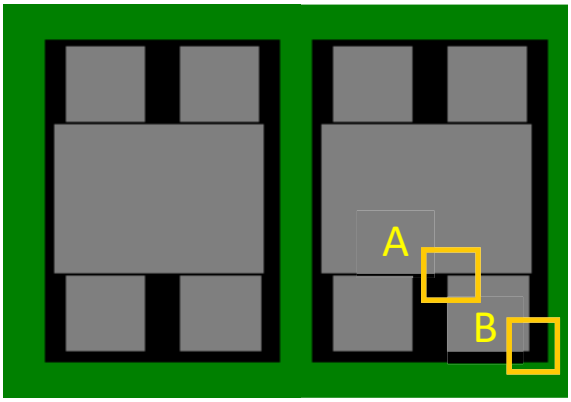


Figure 11. Cross-section locations

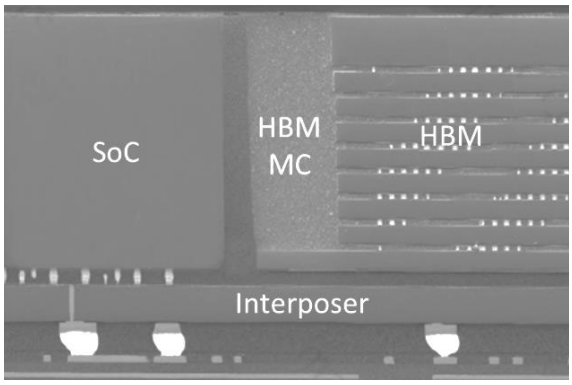


Figure 12. Cross-section of TV1 at location A

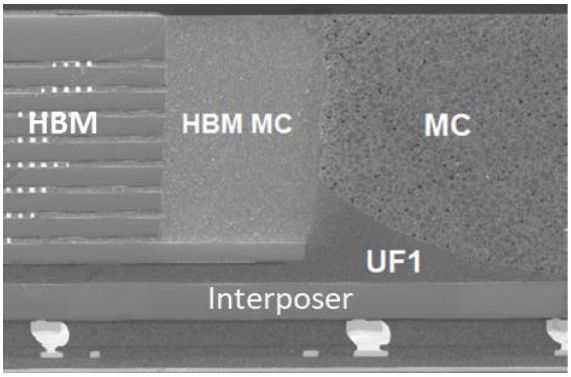


Figure 13. Cross-section at TV1 at location B

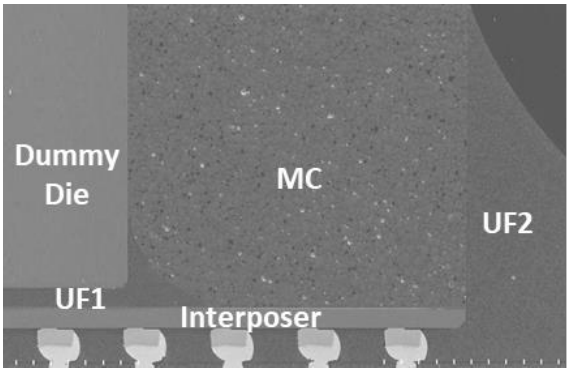


Figure 14. Cross-section of TV2 with thin interposer at location B

IV. Conclusion

The reliability of large 2.5D MCM package designs was evaluated using JEDEC component level stress tests. Our study showed that package stress from thermal cycling could cause underfill cracking at the interposer corner. Package design is an important factor that affects package warpage and reliability. Reducing device corner stress is critical to developing a reliable package. Decreasing the interposer thickness from 100 um to 50 um reduces the module corner stress. Increasing C4 solder joint height also lowers the interposer corner stress and improves package reliability. By optimizing the package structure, the large 2.5D MCM packages were able to pass the JEDEC component stress tests.

Acknowledgment

The authors would like to thank MediaTek's thermal team and TSMC simulation team for their assistance with finite element stress simulations and failure analysis.

References

[1] H.Y. Son, et al., "Mechanical and thermal characterization of TSV multi-chip stacked packages for reliable 3D IC applications." 2016 IEEE 66th Electronic Components and Technology Conference (ECTC). IEEE, 2016

[2] S. Y. Hou et al., "Wafer-Level Integration of an Advanced Logic-Memory System Through the Second-Generation CoWoS Technology," in IEEE Transactions on Electron Devices, vol. 64, no. 10, pp. 4071-4077, Oct. 2017

[3] H. J. Lin et al., "High Reliability Solution of 2.5D Package Technologies", IEEE 23rd Electronics Packaging Technology Conference (EPTC), pp. 620-623, 2021

[4] W. C. Chen et al., "Wafer level integration of an advanced logic-memory system through 2nd generation CoWoS technology." 2017 Symposium on VLSI Technology. IEEE, 2017