

Impact of Dielectric and Copper Via Design on Wafer-to-Wafer Hybrid Bonding

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Abstract—Hybrid bonding is key to achieving high-quality interconnect interfaces for fine pitch integration. It has an advantage over other types of interconnects as it allows a high I/O count for high-density memory, increased power and improved signal speed. To achieve high-quality hybrid bonding, Cu interconnects are embedded in the dielectric. The surface is planarized using chemical mechanical polishing. The final CMP process is usually a two-step process involving copper bulk CMP and then barrier CMP. Barrier CMP leads to the final surface finish which is used for hybrid bonding. The final surface has four key surface properties such as copper recess in the vias known as dishing, erosion and roughness of the dielectric layer, and profile change from high-density copper vias towards low-density copper vias. Most of these parameters are tuned using the CMP process. In this work, we present the impact of dielectric on the metal CMP process and look into the atomic force microscopy (AFM) dishing and roll-off behaviour of the interconnect vias, scaling down from 5 μm pitch to 1 μm pitch using silicon oxynitride dielectric as the bonding dielectric.

Keywords—3D integration, SiP, hybrid bonding, cu-cu bonding, cmp, dishing, roll-off, D2D, D2W, W2W

I. INTRODUCTION

3D integration has enabled the manufacturing of semiconductor packages for application in the internet of things (IoT) [1], image sensors [2], and high bandwidth memory (HBM) [3]. Hybrid bonding technology [4] has been developed for various applications to enable high-density interconnect packaging. Some of the latest technologies developed with hybrid bonding technology are image sensors [5], micro light emitting diode (microLED) [6] and stacked memory for server applications [7]. The advent of mobile computing such as mobile phone and tablets are possible due to heterogeneous 3D integration which has enabled tight integration of systems-in-package (SiP) with increased signal integrity and improved power efficiency. One of the assembly approach to 3D integration for high-density interconnect assembly is by using hybrid bonding technology.

Hybrid bonding technology combines direct bonding technology with embedded interconnect vias leading to copper (Cu)/dielectric bonding. When compared to solid-liquid-

interdiffusion (SLID) bonding, hybrid bonding can provide interconnect technology scaling beyond 10 μm pitch. Thus, enabling pitch scaling with CMOS back-end-of-line (BEOL) with improved alignment tolerances. Hybrid bonding can be applied to three types of stacking approaches, namely, wafer-to-wafer (W2W), die-to-wafer (D2W) and die-to-die (D2D). Of all the approaches, the wafer-level bonding approach is relatively easier when compared to the die level due to compatible equipment availability for wafer-level cleaning and handling. On the contrary, the die-level hybrid bonding approach is difficult to envisage with high yield because of particle contamination that may occur during the dicing and arm movement of the bonder. D2W and D2D also come with additional handling challenges of the die during surface cleaning, plasma activation and bonding leading to yield loss. On the contrary, the advantage of D2D and D2W bonding is that we can get a high yield with pre-electrically tested known-good-dies (KGD).

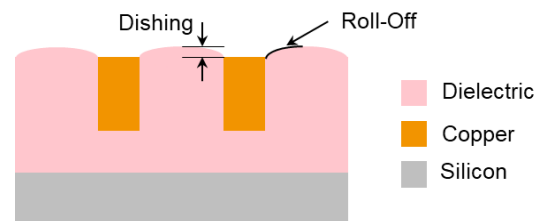


Fig. 1. Surface profile showing dishing and roll-off after metal chemical mechanical polishing.

The standard CMOS damascene process is used to prepare the bonding surface. Surface topography plays a key role to enable high bonding yield. Different via density and pitches can have different via dishing and roll-off of the oxide. “Dishing” (see Fig. 1) is defined as the distance between the dielectric surface and the copper via surface when the copper surface is below the dielectric surface. If the copper via surface is above the dielectric surface then it will be known as “protrusion”. Whether the interconnecting copper via will be in dishing or protrusion depends upon the selectivity between the copper and the barrier/liner layer during the metal chemical mechanical polishing (CMP) processing. CMP is a key technology enabler

for hybrid bonding as it enables extremely smooth and flat surfaces at the nanometer level for effective bond propagation during the low-temperature bonding process. Also, the different dielectrics will have a different impact on the dielectric removal rate during the CMP process. The second important parameter is the “roll-off” of the dielectric between the copper vias which is the slope of the dielectric around the copper via and is measured as nm/ μm . The third key parameter is the surface topography which will define the flatness of the bonding surface for bonding. The surface topography may change with changing density of the copper via pattern.

This paper presents the work done with various dielectrics as the bonding layer, describing the dishing, and roll-off for fine pitch interconnect against various CMP parameters. Finally, showing the excellent bonding results obtained after hybrid bonding.

II. EXPERIMENTS

A. Design

The reticle is designed to enable fine pitch alignment tolerances of up to 200 nm during wafer alignment. The copper density on the test array varies from 12.57 % up to 16 %. The test chip is designed with both square and circular vias. The pitch sizes vary from 5 μm pitch (via diameter 2.25 μm) all the way up to 1 μm pitch (via diameter 450 nm). The area of via array varies as per the pitch, for 5 μm pitch via array, the area is 392 μm x 242 μm , for 3 μm pitch via array, the area is 235 μm x 145 μm , for 2 μm and 1 μm pitch via array the area is 158 μm x 98 μm .

B. Fabrication

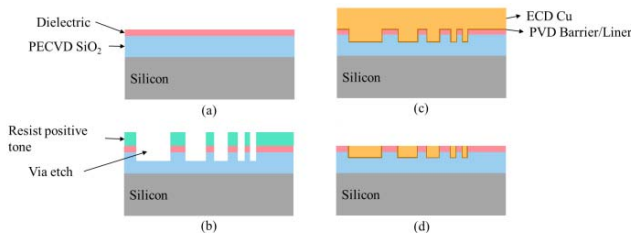


Fig. 2. Schematics of single damascene process, (a) Silicon Oxynitride dielectric (SiON) is deposited on PECVD SiO₂ layer and CMP polished. (b) the wafer is then patterned using positive tone photoresist and then vias are etched using plasma etching. (c) The PVD process deposits barrier/liner/seed and then copper is electroplated to fill the vias. (d) lastly, the wafer is polished by the metal CMP process.

Wafer fabrication steps are shown in fig. 2, The wafers are prepared by deposition of SiO₂ by PECVD at 300 °C and annealed at 350 °C. After this, the SiON bonding dielectric is deposited by the PECVD process at 300 °C. The SiON dielectric is then polished using the dielectric CMP process using IPEC472 by Axus Technology and the roughness is measured using Agilent 5600LS atomic force microscopy. The wafer is then patterned using the i-line stepper lithography NSR2205i11D and etched in an oxford plasmalab system 100 by oxford instruments using reactive ion plasma etching. The barrier/liner/seed layer is deposited by physical vapour deposition (PVD) and then 1500 nm copper is electroplated in ClassOne Solistic. Finally, the wafer is polished for metal

planarization in the Surface CMP tool by Axus Technology. There are two steps to metal CMP technology, the first being the copper CMP which removes the bulk copper up to the endpoint with a certain overpolish time and the second is the barrier CMP which removes the barrier/liner and is also used as the final polishing step to adjust the via dishing. Two wafers are polished for each dielectric type. The bonding is done in the EVG Gemini wafer bonder. During bonding, the wafers are first, treated with low-nitrogen plasma and then rinsed with DIW to generate a hydroxyl group on the bonding surfaces. The wafers are then precisely aligned using the wafer aligner in the EVG Gemini and then bonded at room temperature without any pressure and at room temperature leading to hybrid bonding.

C. Characterisation and Analysis

Before bonding and after the metal CMP process, the wafers are characterized for dishing, roll-off and long scan by Bruker Automated AFM, Insight Cap. The scanning is done at 2048 points/line with 128 lines. The scan size was dependent on the pitch that was scanned. For 1 μm pitch, the scan size was 6 μm x 6 μm , for 2 μm pitch it was 12 μm x 12 μm , for 3 μm it was 18 μm x 18 μm and for 5 μm pitch it was 30 μm x 30 μm . the scan size is decided to capture a 5 x 5 via array for statistical analysis. The automated dishing/roll-off analysis was performed by means of self-made software that uses artificial intelligence for automated via detection and data evaluation [8][9]. The long scan data is analyzed using a similar script that firstly levels the profile with a line and then with a spline curve. The profile is then filtered, the respective maximum and minimum peaks are extracted and statistically, the slope is calculated. After bonding the wafers are characterized using an infrared camera and scanning acoustic microscopy SAM300 by PVA Tepla using a 175 MHz transducer with a focal length of 3.2 mm. To enable high-quality scanning, during SAM inspection the top wafer of the bonded pair is grinded and polished to 525 μm silicon with the top wafer having a silicon thickness of 100 μm .

III. RESULTS & DISCUSSION

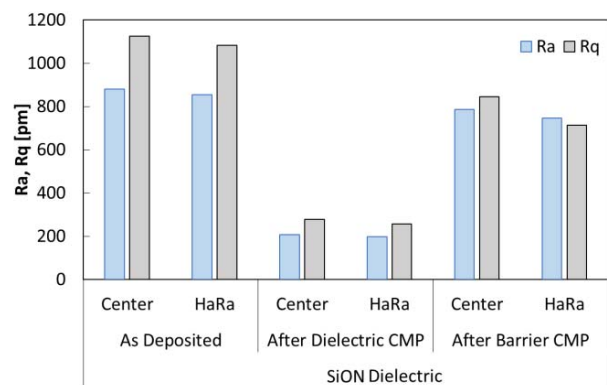


Fig. 3. Roughness of the SiON dielectric surface for as deposited, after dielectric CMP and after Barrier CMP. “HaRa” in the above graph is a short form to “Half-Radius”.

In this section, we present a detailed analysis of the dielectric roughness and wafer geometry change after every process (that

is, dielectric deposition, dielectric CMP and barrier CMP). Bonding surface behaviour (such as, via dishing, dielectric roll-off and surface topography) is discussed after the metal CMP process in sections B and C. Finally, the scanning acoustic microscopy analysis of the bonded wafer pair is shown in section D.

A. Dielectric Roughness

The SiON dielectric is deposited on the wafer and is described in section II-B. To characterize the surface roughness the dummy wafers are also coated with the respective dielectric along with the real wafers. The roughness is measured before and after dielectric chemical mechanical polishing as these are the dielectric bonding surfaces. As deposited dielectric show roughness (Ra) to be less than 1 nm. After dielectric CMP the roughness decreases to less than 300 pm. The low roughness value suggests lower mechanical asperity and higher chances of good bond formation. Again, we have to be careful that the dielectric surface may become rough during the barrier CMP as the roughness will depend on the size of the slurry particle used for the barrier polish and it is observed that the roughness increases to 800 pm (approx.) after barrier CMP.

B. Dishing and Roll-Off of the Cu Via after metal CMP

The barrier CMP is done on the same pad as the Cu CMP for a pre-calibrated time, head pressure and slurry flow. With barrier CMP the dishing and roll-off values will depend on the removal rate of the copper versus the removal rate of the barrier/liner and the dielectric. Fig. 4 shows the copper dishing, dielectric roll-off and the dishing range results after barrier polish as measured with the AFM. The discussion regarding the results (see Fig. 4) obtained after the metal CMP can be further classified into 2 parts depending upon the dishing values.

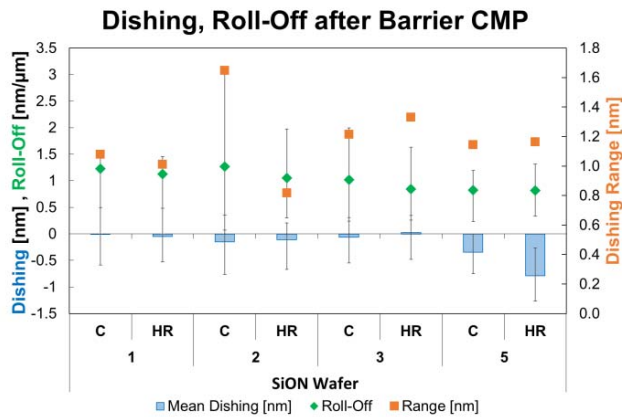


Fig. 4. The above graphs show the dishing, dielectric roll-off and the dishing range for 5x5 via array for, 1 μm, 2 μm, 3 μm, and 5 μm via pitch respectively. “C” stands for measurement at the center of the wafer and “HR” stands for the measurement at the half-radius of the wafer.

All the via pitches (that is, 1 μm, 2 μm, 3 μm and 5 μm) after hard pad barrier CMP are in dishing. The results show very good dishing control for all via diameters. The via dishing behaviour is very similar at the centre and a half radius of the wafer which suggests a good CMP control across the wafer. The large dishing value of 5 μm pitch vias when compared to 3

μm, 2 μm and 1 μm pitch vias can be compensated with the copper expansion of the large copper volume available in the large vias as $\delta l \propto V(Cu)$, where, δl is the copper expansion in the via and the $V(Cu)$ is the volume of copper available in the via.

The roll-off measurement on SiON is 1 nm/μm across all the via pitches, suggesting a very flat dielectric between the vias. The roll-off variation is large at the centre for 2 μm pitch but for the rest, the variation is within +/- 1nm/μm. Usually, as the pitch size increases the roll-off also increases. The roll-off behaviour at the centre and half-radius is similar. Lower roll-off values will lead to better bond propagation and hence higher bonding yield.

C. Topography

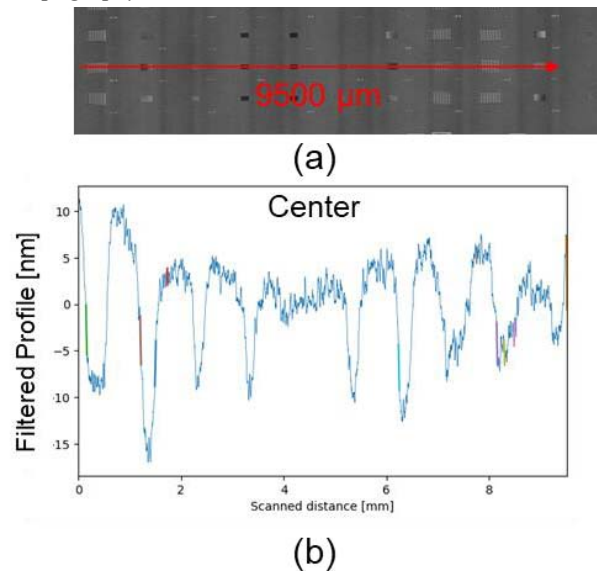


Fig. 5. AFM topography scan a) the scan length and the structures scanned for the topography profile. The long scan profile over b) profile at the centre of the wafer after barrier CMP.

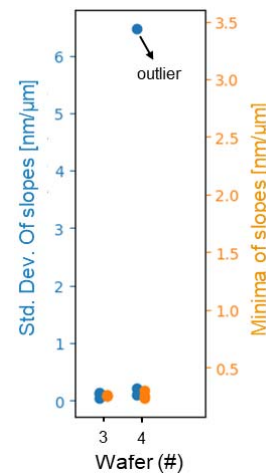


Fig. 6. The statistical value of the slopes obtained from the long scan topography measurement for the top (wafer 3) and bottom (wafer 4) wafer.

The wafer was scanned with long scan measurements for a possible surface topography that may play a major role in dielectric bonding. Fig. 5(a) shows the scan length and the scanned structure using AFM for surface topography. The SiON show a very low change in the profile of +/- 5 nm. From the topography measurement, we can see the impact of copper density and the size of the array. The structure array area shows an impact on the recess depth during the topography measurement. When comparing the slope of the recess (see Fig. 6) SiON dielectric shows a slope of less than 1 nm/ μm . For 3 μm via arrays, the topography recess is deeper than for 2 μm , and 1 μm via array. For 5 μm via array, it can be deeper but this is compensated by a large array size.

D. Hybrid Bonding

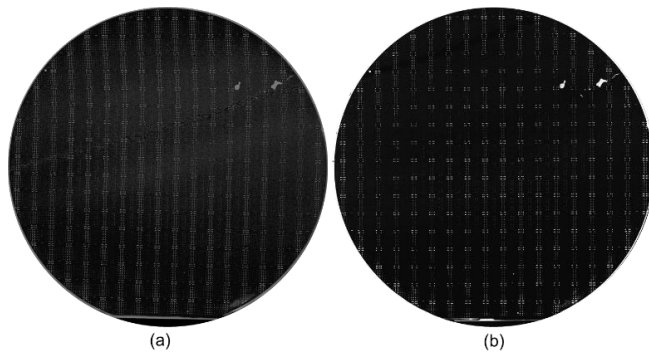
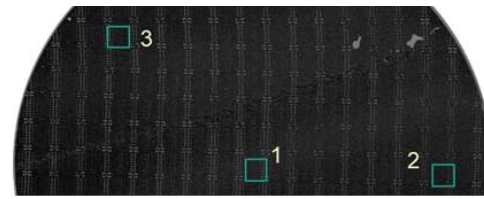
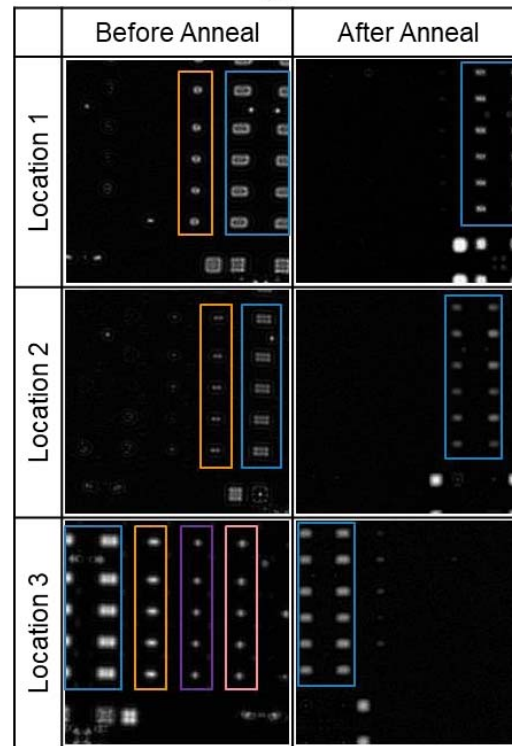


Fig. 7. Scanning acoustic microscopy images of the bonded wafer pair, a) after room temperature bonding, b) after annealing.

The wafer pairs are bonded at room temperature and because of the topography in the via structure (see Fig. 5), we can expect non-bonded regions between the bonded dielectrics (see Fig. 7 and Fig. 8). By fine investigation of the via arrays it is observed that 5 μm and 3 μm pitch via arrays do not show bonded and this can be seen by bright white regions (Fig. 8) under before annealing column. The bonded wafer pair is annealed at 95 $^{\circ}\text{C}$ for 20 min to evaporate any water present at the edge of the wafer then at 200 $^{\circ}\text{C}$ for 120 min to improve the bond strength between the SiON dielectric and then at 350 $^{\circ}\text{C}$ for 60 min to enable copper expansion of copper vias and formation of interconnects between the wafer pair. After annealing, it is observed that the bonding yield has improved in respective locations. Location 1 and location 2 show 100% bonding yield for 3 μm pitch via array (in the orange square) and a decrease in the non-bonded region for 5 μm pitch (in the blue square) via arrays. Location 3, shows non-bonded regions for all pitches via arrays and this has improved significantly after anneal. From the wafer geometry inspection of the wafer before and after anneal we can observe a reduction of 22% in the wafer bow after annealing and subsequent improvement in wafer warp and sori of the bonded pair.



(a)



(b)

Fig. 8. a) location of detailed SAM inspection b) SAM of via arrays before and after annealing. The blue, orange, purple and pink square shows 5 μm , 3 μm , 2 μm and 1 μm pitch via arrays respectively.

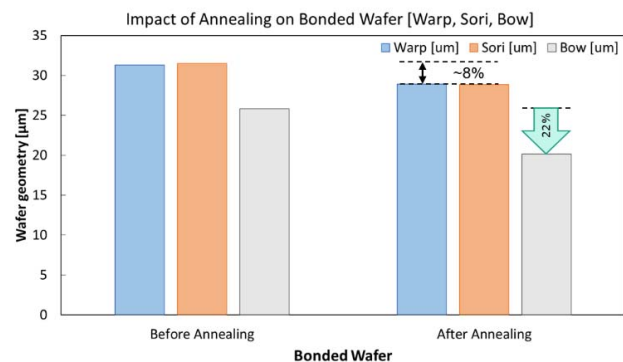


Fig. 9. Impact of annealing on wafer geometry.

IV. CONCLUSION

In this paper, we propose the following key learnings with regard to hybrid bonding when using SiON as the bonding dielectric layer.

- Dielectric roughness increases after barrier metal CMP which may lead to stochastic regions of poor bonding.
- SiON shows lower roll-off, and narrow dishing across all via pitch sizes and arrays.
- Topography inspection shows the impact of via density as well as the array size on the recess of the structured region.
- Annealing can significantly improve the bonding yield for smaller arrays. 5 μ m pitch via arrays shows a decrease in the non-bonded region after annealing.
- Wafer warpage and bow also is affected by the annealing and show a further decrease.

Hence, from this work, we demonstrate the impact of via array size and density on the hybrid bonding yield. SiON shows uniform dishing and topography across different copper density and pitch sizes and therefore can be used as a promising bonding material for high-density interconnect formation via hybrid bonding technology.

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