Extremely Large 3.5D Heterogeneous Integration for the Next-Generation Packaging Technology

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***Abstract*—2.5D silicon interposer for multi-die heterogeneous integration is the mainstream package architecture for a high-performance computing (HPC) and an artificial intelligence (AI) application. In this study, 3.5D package is demonstrated to combine 2.5D silicon interposer and 3D architecture to obtain high-performance and high-density interconnection with the small footprint system package. Extremely large Si interposer (4x reticle size) was manufactured and integrated with multi logic test chips with 12-HBMs, 3-chiplets and 3D-ASIC. 3D-ASIC was manufactured by vertical interconnection of two partitioned chips by Cu-Cu hybrid bonding. 3D-ASIC will be able to overcome effectively the single chip reticle size limitation and large die yield issue in Si fabrication. Furthermore 12-HBMs and 3-chiplets were assembled on silicon interposer using Chip on Wafer (CoW) process for higher system bandwidth. 3D-ASIC was attached on silicon interposer by solder reflow bonding process with 40um bump pitch. To avoid underfill void on narrow chip gap and die to die space, vacuum devoid process was introduced and the underfill void under multi-chip was completely removed. The extremely large molded Si interposer with multi-die was assembled on organic substrate successfully showing the reliable joint quality by controlling molded Si interposer and substrate warpage effectively. The interfacial stress between various multi-heterogeneous chips was analyzed through finite element method (FEM) simulation and the impact on reliability will be discussed.**

Keywords—2.5D, 3D, 3.5D, Si interposer, 3D ASIC, Heterogeneous integration, Reliability

I. INTRODUCTION

The latest wave of technology evolution is based on artificial intelligence, cloud computing, and autonomous driving [1]. These leading edge technology has been built by the semiconductor and packaging technology development for more than Moore's law [2]. In this development, 2.5-dimensinal (2.5D) packaging has been a key role of the high speed and performance to overcome the bottle-neck of the bandwidth between memory and application specific integrated circuits (ASICs). On the silicon interposer, the homogenous and heterogeneous dies are integrated and connected for high speed and performance required by the system.

2.5D packaging technology has rapidly developed with the larger silicon interposer fabrication, chip on wafer (COW) assembly process, and packaging materials in accordance with these market demand as shown in Fig. 1. Even though a great progress of 2.5D silicon interposer size to 52mm x 55mm (2860mm^2) to capable to have 2-ASICs and 8-HBMs has been implemented, the silicon interposer size is expected to increase more to integrate the more multi-chips on it in the future. The larger silicon interposer have still many assembly challenges in the packaging process such as the warpage control for bump joint between larger molded Si interposer and substrate, the underfill void, and even the package reliability issues. In addition, as it is required the more multi-functional blocks to make the higher processing speed and lower latency of them as monolithic device for the high end application, the ASIC chip size is expected to be more increased and the production yield of ASICs could have serious problems in the silicon fabrication because of the more difficulty to avoid particle contamination on it.

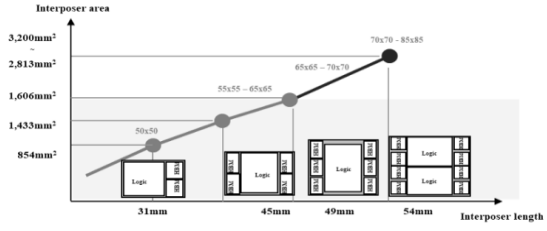

Fig. 1. 2.5D deveoplemnt trend of the silicon interposer size [3].

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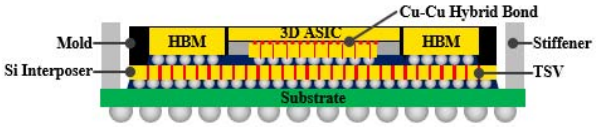
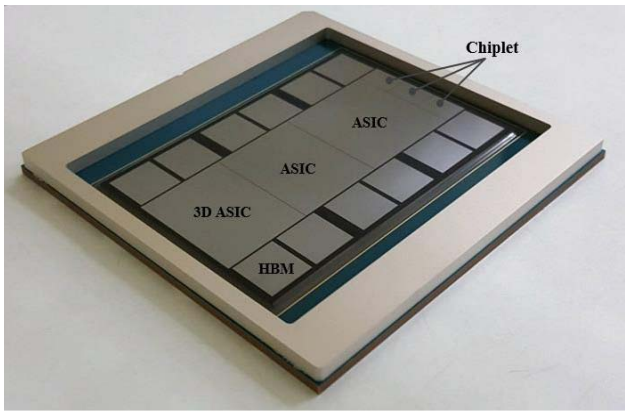
To break through the limits of these problems, 3.5-dimensional (3.5D) packaging has been initiated, which is a fusion of 2.5-dimensional (2.5D) and 3-dimensional (3D) packaging for next advanced packaging technologies.

3.5D packaging is a technology which is integrated 3D stacking chips connected with a through silicon via (TSV), arranged horizontally and connected by a silicon interposer such as 3D-ASIC, HBMs, and 3D multi-chips. It is expected to reduce ASIC size and even the silicon interposer size in the physical dimension because their vertical stacked dies are partitioned by functional blocks and interconnected directly by Cu-Cu hybrid bonding to sustain the performance as one monolithic device. Moreover, in the production, the smaller ICs is expected to show the high yield so that it will reduce the fabrication cost for the market requirement.

In this paper, 3.5D packaging were studied and demonstrated with the optimization with the assembly process and materials on the extremely large silicon interposer as shown in Fig. 2. Silicon interposer was integrated with 12-HBMs, 3-chiplets, and 3-ASICs. One of ASICs was vertically stacked with two chips which are partitioned by its functional blocks. Each chips was stacked face to face interconnected with Cu-Cu hybrid bonding technology which enable to connect directly between chips. Many kinds of the multi-chips were arranged horizontally and interconnected by micro bumps on the extremely large silicon interposer. Wafer level underfill material was filled in the underneath the multi-chips through the narrow space between chips. The interfacial stress between various multi-heterogeneous chips was analyzed through finite element method (FEM) simulation and the impact on reliability will be discussed.



(a)



(b)

Fig. 2. The 3.5D package structure. (a) Schematic vertical structure and (b) Tilt view of package structure.

II. TEST VEHICLE INFORMATION

3.5D test vehicle was consisted of 3-ASICs, and 3-chiplets, 12-HBMs on the silicon interposer as showed on Fig. 2(b). The ASIC chip size was 25mm x 19mm. The ASIC was designed as a test chip for testing connection on silicon interposer chips with daisy concept. One of ASICs at the south side of the silicon interposer was 3D stacking chips which is connected with Cu-Cu Hybrid bonding with 4um pitch. The schematic structure of 2 chips stacked in the ASIC was shown in Fig. 3. Top silicon chip size is larger than the bottom silicon chips. To form micro bump on the small chips, the oxide was filled with the gap around small chip and then polished the surface to expose the TSV structure on it by chemical and mechanical polishing (CMP). Metal lines were made it followed by that. Micro bumps of each ASIC is designed at 40um pitch and the number of it is 170,000. To detect the connection of its internal side electrically, the daisy chain of ASIC chip was connected by Cu-Cu hybrid bond to micro bump through TSV.

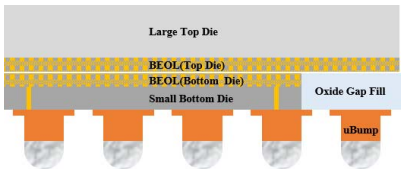


Fig. 3. Schematic vertical structure of the 3D ASIC chip to interconnect with Cu-Cu hybrid bonding.

The silicon interposer was designed to be enable for arrangement of 3-ASIC, 3-chiplets, and 12-HBMs. The gap of the each chip was 60um to ensure the electrical characteristics when the chips were connected internally for signal processing. Chiplet size was 8.4mm x 6.0mm and its micro bump pitch is 50um. The number of Cu pillar bumps on the chiplet is about 11,000. HBM was the generation 3 (Gen3) and was arrayed the both sides of the each ASICs to interconnect these as the shorter distance for the high speed processing between them. The HBM Gen3 size is 11mm x 11mm. The HBM was stacked 8 core dies on the buffer die in it. The bump pitch of buffer die was the minimum 73um. Substrate was made by a build-up process and the number of its layers were 14(6-2-6). To control the warpage of the larger substrate, extremely lower coefficient of thermal expansion (CTE) core material was used and the Cu layer design was optimized. Stiffener foot width was 10 x 3.5mm and its height was thicker than the substrate thickness to control package warpage after stiffener attached process. The table. 1 was summarized the test vehicle structure and materials of test vehicle.

TABLE 1. TEST VEHICLE INFORMATION: STRUCTURE AND MATERIAL

Structure/Material	Chip Size (mm)	# of Bump	Pitch (um)	Remark
ASIC (3D ASIC)	25 x 19	170,000~180,000	40	-
Chiplet	8.4 x 6.0	10,000~11,000	50	-
HBM	11 x 11	7000~8000	73	HBM3 (Generation3)
Substrate	-	-	-	Layer : 14(6-2-6)
Stiffener	-	-	-	Foot width : 10mm x 3.5mm

III. PROCESS FLOW OF ASSEMBLY

The 3.5D assembly process is based on CoW process. A silicon interposer wafer with TSV was attached 1st glass carrier with the glue to handle thin silicon interposer during the process. TSV was exposed after removing thick silicon by a grinding and a silicon etch process. The final silicon interposer thickness was to 110um on the 1st glass carrier. And then, the Cu pillar bump was fabricated on the silicon interposer back side. A 2nd glass carrier was attached on backside of silicon interposer with thick glue coating layer to cover Cu pillar bump. And then 1st carrier was detached from silicon interposer to interconnect heterogeneous dies on its pad. ASICs, chiplets, HBMs were arranged on the silicon interposer by flip chip bonder and interconnected the bump of heterogeneous dies to the pad of silicon interposer by a reflow process. In order to protect the micro bump joint, wafer level underfill process was applied. Various heterogeneous chip sizes and spaces made it difficult to control a uniform front flow of underfill. It caused to make the flow turbulence in the filling process by the capillary effect so that a devoid process was also applied it by vacuum, which is followed pressured curing process to remove the void during underfill cure. For a void inspection, scanning acoustic tomography (SAT) equipment was used after its curing.

The encapsulation was formed on wafer and removed partially on top of the wafer to expose the silicon back side of heterogeneous dies which a heat sink was attached directly for heat dissipation in the system level assembly. To support a molded wafer in the 2nd carrier detach process, the molded wafer was mounted on the dicing tape attached 400mm ring frame and then 2nd carrier and glue was removed mechanically, which is followed by cleaning the Cu pillar bump of the molded wafer by chemical etchant and remove the glue remained. The molded wafer was separated into a molded chip module by dicing. To form high quality joint between substrate and dies by a reflow process, a molded chip module should be matched with substrate behavior and were within its warpage specific value in the differences above the soldering temperature. As the size of the molded chip module increases, material optimization is essential to control the warpage gap between the chip module and the organic substrate. The warpage of a molded chip module and the organic substrate were measured by shadow moiré from room temperature to 240℃. For the analysis, their warpage value and its joint quality were compared after a reflow process. To check the interconnection quality of molded chip module on the substrate, samples were grinded and polished in the cross-sectioned form and inspected by optical microscope.

The underfill dispensing was followed then. A stiffener was attached on the substrate with an adhesive to control the package warpage. After that a solder ball was applied using a reflow. The schematic assembly process flow of 3.5D was showed in Fig. 4. A thermal cycle test was done to identify the internal stress of heterogeneous dies in the extremely large 3.5D package. Temperature range was from -40 to 125℃ duration 2 cycle per 1 hour. Electrical test was done to find a failure. Finite element method (FEM) simulation was also done to compare its internal stress at T-zone which is located between ASICs and HBMs.

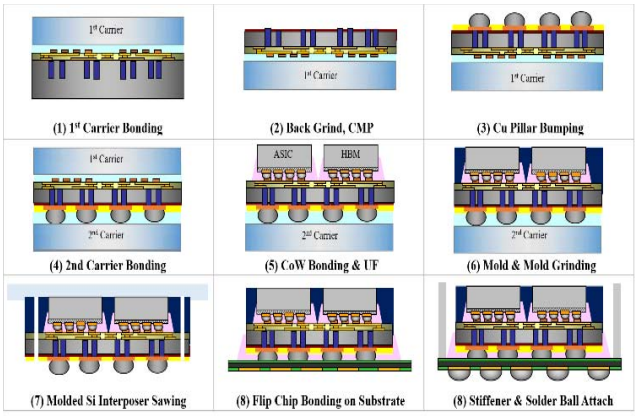


Fig. 4. Fabrication process flow of 2.5D assembly.

IV. RESULTS AND DISCUSSION

A. The result of underfill with the heterogeneous dies

Underfill dispensing pattern was modified to fill the narrow gap of separate multi-dies. The larger space and the more chip gaps between heterogeneous dies made it difficult to flow the underfill uniformly from the entry site to exit site by capillary force during a dispensing process. Because the cavity between dies was also filled with underfill, which made void traps in the front flow of underfill. To make uniform flow of underfill, the dispensing process was performed a top of the ASIC dies as shown in Fig. 5. The shorter length of the flow showed less void trap after dispensing.

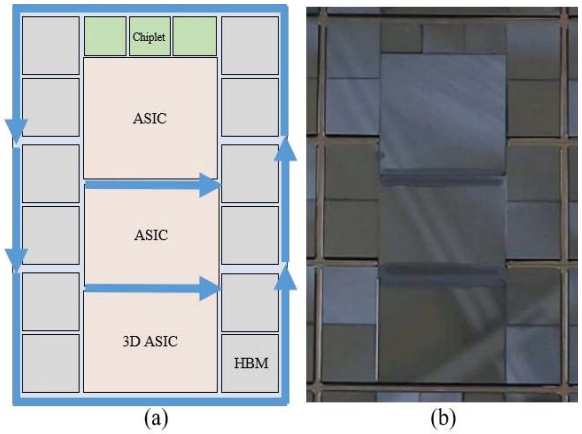


Fig. 5. (a) Optimized underfill dispensing pattern for filling multi-dies and (b) Appearance after underfill dispense.

To remove void traps, de-void process was applied by vacuum after the underfill dispensing. The vacuum was able to squeeze out the void from underfill because the viscosity of underfill was still lower before the underfill cure process. When the pressure went below the 1 atm, the void in the underfill was moved through the materials and squeezed out. Fig. 6. showed the exit appearance of the void on the die after vacuum process.

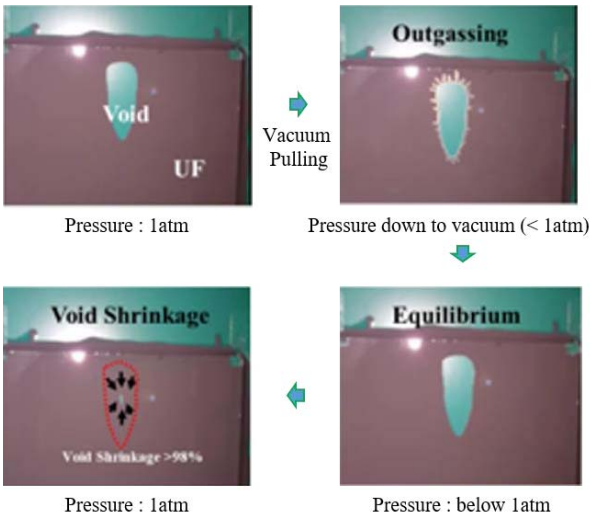


Fig. 6. Void squeeze out images after a vacuum process.

The inspection results of the void by SAT after pressure cure showed in Fig. 7. The vacuum process was required to remove all the underfill voids of the heterogeneous chips integrated into the Si interposer perfectly.

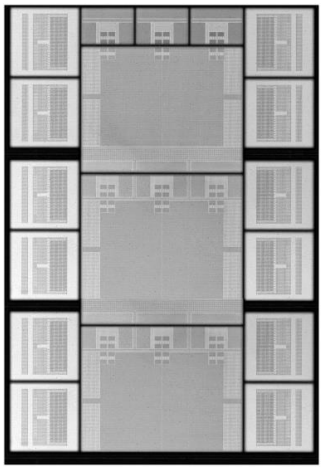


Fig. 7. Underfill void inspection results by SAT after pressure curing process.

B. The bonding result of an extremely large molded chip module on a substrate in the reflow process.

To make bump joint between molded chip module and substrate, their warpage was controlled by their effective gap at the soldering temperature. As optimized the materials of substrate and design of a molded chip module, their warpage result showed in the Fig. 8. Because of its increased size, the warpage of a molded chip module showed the 135um at 240℃. The warpage value was changed from 49um to -7um at the solder solidification temperature from 217℃ to 186℃. The optimized substrate warpage was measured and showed the slight change around 50um at the solder solidification temperature. As the result of that, the effective gap between the molded chip module and the substrate was showed from 30 to 64um during the solder temperature.

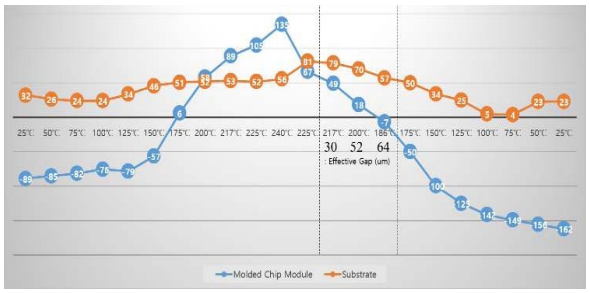
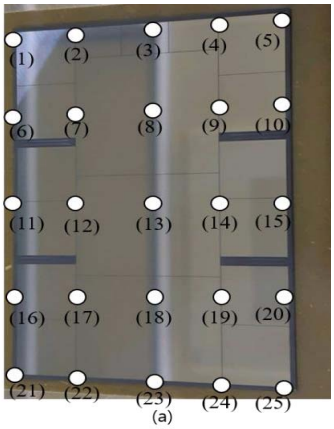


Fig 8. The results of the moiré warpage of the molded chip module and substrate warpage.

The Cu pillar bump joint was formed by a reflow process. And then sample was analyzed by cross section and observed the joint formation measuring joint gap height by optical microscope. The results of the Cu pillar joint gap showed in Fig. 9. Joint gap height showed the average 67um and no joint failure such as non-wet and short. As the sample was sectioned and observed by an optical microscope, the Cu pillar joint was formed the stable interconnection as shown in Fig. 10. Compared the effective gap with joint gap height, the similar value was showed. With these result the effective gap is considered a main control factor to make the Cu pillar bump joint in the large silicon interposer bonding.



(1)	67	(2)	77	(3)	71	(4)	74	(5)	66
(6)	64	(7)	59	(8)	62	(9)	68	(10)	65
(11)	63	(12)	66	(13)	59	(14)	64	(15)	68
(16)	67	(17)	65	(18)	60	(19)	67	(20)	70
(21)	67	(22)	73	(23)	72	(24)	75	(25)	67

(b)

Fig. 9. The results of the Cu pillar bump joint gap height after reflow bonding. (a) Measurement location and (b) Joint gap height.

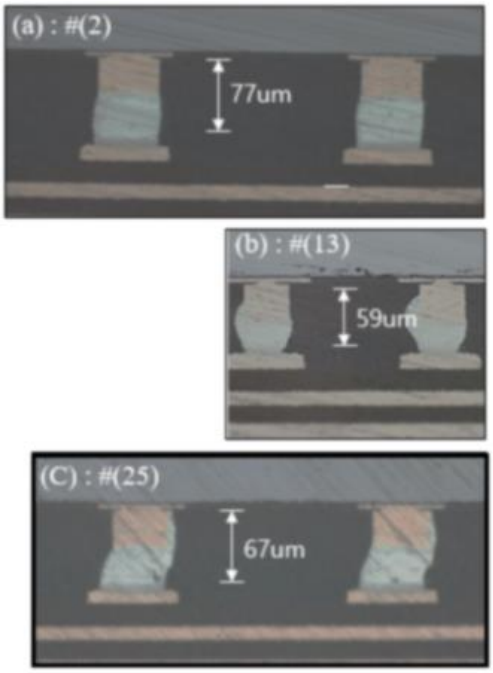


Fig. 10. Cross section images of Cu pillar bump joint on the location of chip module. (a) #2(top left), (b) #13(center), and (c) #25(bottom right)

C. The results of the assembly and thermal cycling test

First, a cross-sectional analysis was conducted to confirm the quality of the product before the reliability evaluation. Because many types of chips, including 3D chip, were stacked in 2.5D structure, it was checked whether there were any failures such as delamination or voids during the assembly processes and shown in Fig. 11. The quality of Cu-Cu hybrid bonding interface between the top and bottom die of the 3D chip was checked without any voids and delamination. Finally it was confirmed that there is no failure such as joints between heterogeneous chips and Si interposer including 3D chip, underfill and mold encapsulation delamination, and bonding quality between molded chip module and organic substrate.

FEM analysis was conducted to verify the structural reliability stress risk point of the heterogeneous 3.5D structure including 3D chip, and reliability evaluation was conducted with fabricated samples. The stress risk point in the thermo-mechanical environment was analyzed. As a result, as described in Fig. 12, it was analyzed that the T-zone where the 3-chips stacked adjacent to each other was the most vulnerable to thermo-mechanical stress. Thermal cycling test after the pre-condition MSL3 was conducted followed by the JESD22A-104F [4]. The reliability evaluation results are shown in Table 2. MSL3 and TC700cycle were passed without any failure, and the crack was confirmed at the underfill of T-zone at TC1000cycle in Fig. 13. This is consistent with the results predicted by the stress simulation. Though the underfill crack was confirmed by optical microscope investigation, the electrical test was passed because the crack did not propagated to the bottom of the chip and the uBump joint interfaces. Further research is needed to reduce the stress in order to develop a more robust 3.5D structure.

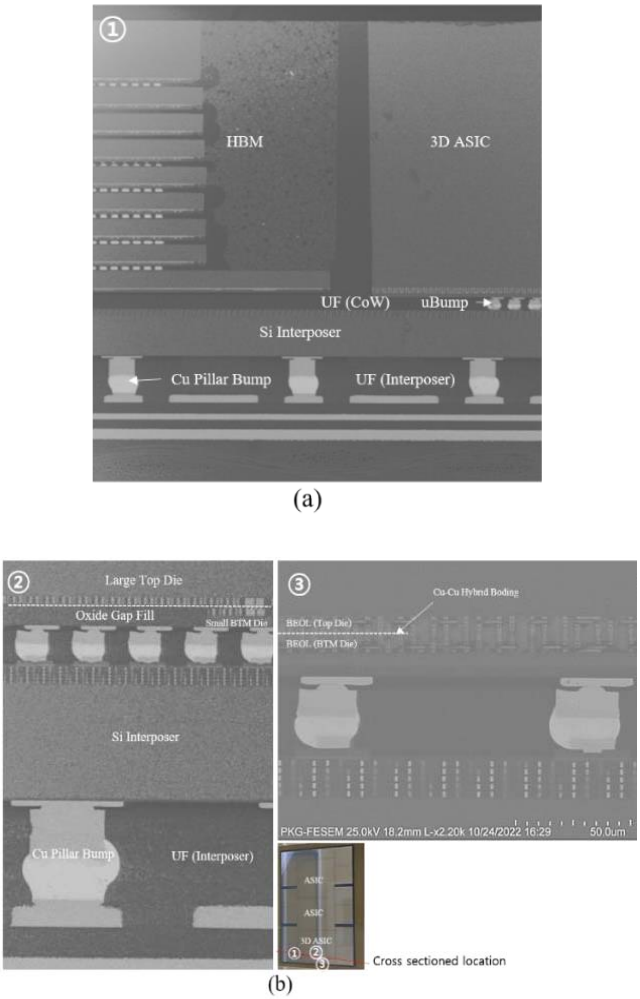


Fig. 11. Cross-section images of Cu pillar bump joint on the location of chip module. (a) #(2), (b) #(13), and (c) #(25)

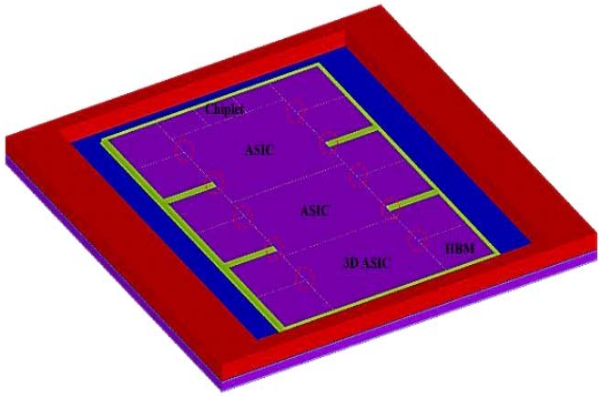


Fig. 12. FEM simulation model of the 3.5D Package.

TABLE 2. RELIABILITY TEST RESULTS

MSL3	TC300cy	TC700cy	TC1000cy
0F/30	0F/30	0F/30	27F/30

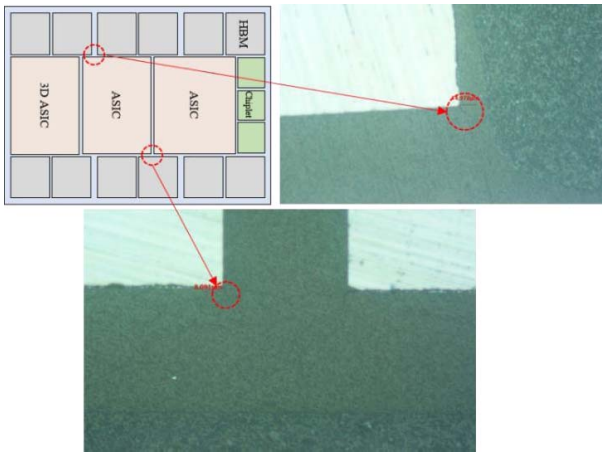


Fig. 13. T-zone underfill crack at TC 1000cycle,

V. CONCLUSION

In this work, 3.5D package was fabricated and studied on the extremely large silicon interposer in terms of assembly process and reliability. A vacuum devoid process is essential to remove UF void when various multi-dies were integrated on the silicon interposer. The effective gap between the molded chip module and the substrate is considered a main control factor to make the Cu pillar bump joint without any failure such as non-wet and short in the large silicon interposer bonding to substrate. T-zone where the 3-chips stacked adjacent to each other was the most vulnerable to thermo-mechanical stress, especially in the T-zone around the ASIC chips and all UF cracks occurred in the T-zone at TC1000cycle as prediction by the stress simulation. As further research, applying lower substrate CTE materials and higher toughness underfill materials to 3.5D package structure are underway.

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