Signal Integrity Co-Design of a High-Speed (20 Gbps) Analog Passive CMOS Switch

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Abstract—A switch (digital or analog) is an integrated circuit (IC) that connects and disconnects an electrical circuit or two separate subsystems. Switches are one of the most ubiquitous electrical circuit components today. However, with broad applications covering multiple market segments, meeting device performance requirements are becoming challenging. Analog switches, configured as multiplexers (mux) or demultiplexers (demux), are designed to pass or isolate analog signals by switching on and off CMOS transistors. However, designing high-performance, high-speed (> 20 Gbps) bi-directional analog CMOS-based passive switches to support system-level end-to-end signal chains is typically plagued by signal integrity and timing issues. Common issues observed in high-speed analog passive switches design are meeting bandwidth, insertion loss, return loss, channel-to-channel crosstalk, OFF isolation, and THD+ (total harmonic distortion) noise. Additionally, the drive for continued miniaturization and highly-integrated switch exacerbates electromagnetic interactions between the system components (i.e., silicon + package + PCB). As such, signal integrity issues are aggravated with a potential impact on system performance if not considered and addressed early in the design phase. This paper presents the package-PCB system electrical co-design and measurement validation results of an analog passive CMOS Mux/Demux device that can support high-speed differential data transmission. We detail how electrical co-optimization of the package-PCB system interaction was achieved through a coupled circuit-to-electromagnetic modeling and simulation methodology. Laboratory measurements on a 4-Channel 20 Gbps Differential 2:1/1:2 Mux/Demux IC are presented that validate the integrity of the co-design modeling and simulation methodology.

Keywords—analog, CMOS, co-design, high-speed, modeling, passive switch, signal integrity

I. INTRODUCTION

The advent of artificial intelligence, machine learning, and cloud computing has increased the amount of processed data. As a result, fast and reliable signal switching is essential for efficient data communication and resource sharing. Fast signal switching is achievable using a high-speed bidirectional passive switch, both in a multiplexer (mux) and demultiplexer (demux) configurations that can switch between high-speed signals with ease and precision. The analog differential passive mux or demux works for high-speed differential interfaces for data rates up to 20 Gbps, including PCI Express 4.0. They are designed to work with various high-speed interfaces, including PCIe, USB, SATA & Display ports. In many PC and server motherboards, the CPU does not have the appropriate number of PCIe channels to provide desired system flexibility for end customers' applications. This device can be used in such applications to switch PCIe TX and RX lanes between two slots.

Recent trends in analog switch design employ switches with FDSOI technology, enabling it to be used for higher frequencies but comes at a higher solution cost [1], [2]. Therefore, one of the biggest design challenges is meeting the same performance (i.e., bandwidth, insertion loss & return loss) of the FDSOI analog switches using traditional bulk CMOS technology. Additionally, the integrated circuit (IC) package and printed circuit board (PCB) parasitics play a critical role in meeting these performance requirements. As a result, signal and power integrity issues are exacerbated with an impact on system performance if not considered and addressed early in the design phase [3-4].

This work details the challenge of achieving a high-speed (20Gbps) analog passive CMOS switch. Section II covers the CMOS-based passive switch's key functional features comparable to FDSOI process technology. The package and PCB physical co-designs and their interactions, along with a description of the system setup, are discussed in Section III. Section IV comprehensively outlines the predictive signal integrity modeling methodology developed to design the package optimally and PCB, and their electromagnetic interactions, to meet or exceed the system-level performance specifications. Finally, a comparative assessment of the modeling methodology compared to empirical measurements of the device system performance is provided. Findings, observations, and future work are also outlined.

II. ANALOG PASSIVE SWITCH DEVICE DETAILS

A. Device Functional Block Schematic

The device under test (DUT) discussed here is a high-speed bidirectional analog CMOS passive switch with four channel 2:1 mux/ demux configurations (see Fig. 1). The critical functional features that enable high-speed competitiveness are CMV tracking, charge pump, gate driver buffer, and IO layout parasitics impact.

B. CMV Tracking

The device supports differential signaling with a common mode voltage range (CMV) of up to 0 to 1.8 V and differential amplitude of up to 1800 mVpp. The adaptive CMV tracking feature ensures that the average voltage level is maintained as the signal switches between different channels. This feature is
essential to maintain signal integrity and accuracy. The analog switch with adaptive voltage tracking technology can support applications where the common mode differs between the RX and TX pair. The device has a weak pull-down of 1MΩ from D [0/1/2/3] [P/N] pins to GND. While these resistors bias the device data channels to a common mode voltage (CMV) of 0 V with very weak strength. But, in typical applications, the device is biased from either side of the device to a valid value (in the range of 0 - 1.8 V).  

C. Charge Pump  
A charge pump is needed to provide a constant overdrive for the switch to meet the high-speed AC performance and the drain-to-source \(R_{DSON}\) across all the supply and Common Mode ranges as shown below:

- \(V_{CM} = 0\) to 1.2V for \(VCC = 1.62V\) to 1.98V
- \(V_{CM} = 0\) to 2V for \(VCC = 2.97V\) to 3.63V

D. Gate Driver Buffer  
The gate-to-source voltage, \(V_{gs}\), of the transistor depends on the input signal swing. For high signal swing, the average channel resistance becomes high. This can be avoided by adding a gate resistance (\(R_g\)) for the active switches. This also allows gate-source and gate-drain capacitances to remain nearly constant during the entire signal period, thereby reducing the dependence of signal swing on channel resistance \(R_{ds}\) and improves the linearity. Figure 2 below shows a schematic of the parasitics associated with the switch.

![Fig. 2. Equivalent small-signal model of switch with associated parasitics.](image)

Rb is the substrate resistance associated with the transistor. To reduce the insertion loss, Rb should be neither zero nor infinite. The appropriate value is chosen to meet the requirements. Shunt paths improve the isolation, providing a low-impedance path for the undesired signal to the RF ground. Each device channel comprises a CMV tracking, charge pump, gate driver, shunt transistors, and the SPDT switches. The multiplexer (Mux) consists of single pole double throw (SPDT) switches that can support up to 20GBps [5]. Switch size is optimally done to meet the requirements for \(R_{on}\) and insertion loss. Circuit techniques are also implemented to support high frequency data with minimal signal integrity issues.

Critical parameters of the high-speed passive switches are bandwidth, insertion loss, return loss, cross talk, ON resistance, and OFF isolation. The switch parasitic influences these parameters - drain-source, drain bulk, and source bulk capacitance), ESD capacitance, routing parasitic, package parasitic, and board parasitic. These are comprehended in the final reduced order Spice model of the IO transistor.

E. IO Routing Parasitics  
The top metal signal routing parasitic (R, L & C) are among the most significant contributors to high-speed performance. Top-level metal layers are used for routing to reduce parasitics. Skin-effect must be reduced in the metal routings between the switch and pins. Appropriate bond pads are chosen to minimize parasitics and improve AC performances. Peak view parasitic extraction provides more accurate modeling of routings at RF frequencies which accurately determines the AC performance. Its silicon signal traces are matched for optimal intra-pair skew performance (Fig. 3). The steps described above ensure the highest accuracy of the IO models to achieve optimal system-level performance.
III. SYSTEM SETUP & DETAILS

The device is an analog 4-channel high-speed Mux/Demux type of switch that can be used for high-speed routing signals between two locations on a circuit board. The device is protocol agnostic and can be used for many high-speed interfaces. The example shown below is for an eight-lane PCIe lane muxing application (Fig. 4).

The device is a passive mux/demux component that does not provide any signal conditioning. However, a specific board implementation has too much loss from CPU to PCIe CEM connectors. In that case, a signal conditioning device such as a linear re-driver might be required for the utmost fidelity of the PCIe link.

The package was designed with optimal high-speed design considerations. The package design must ensure that the bond wire parasitic capacitance is small so that the bandwidth is not limited and insertion loss/return loss is not degraded. Return loss is also improved by adding multiple down-bonds, which enhances the return path. A 3D picture of the package is shown below.

The appropriate width of bond wires is evaluated to optimize the various AC performances. In addition, mutual inductance was increased between the differential signals’ bond wire (placed closely) to improve the return loss. The device is packaged in a 42-pin WQFN RUA package (Fig. 5).

The evaluation module (EVM) PCB was designed with the highest signal integrity routing design considerations. The interconnects were modeled, simulated, and parasitics models were extracted to simulate the impact on the AC parameters. All of these parasitic need to be modeled and brought into the simulation environment to get the AC parameters of the device accurately. Figure 6 below shows a 2D picture of the final designed EVM.

Once the silicon routing, package and PCB designs have been designed optimally, the next step is to the modeling, extraction, and analysis of the whole system. In the next section, a predictive modeling methodology is developed for that purpose.
IV. CO-DESIGN MODELING FLOW

A coupled circuit-to-electromagnetic methodology was developed to assess the overall signal-integrity electrical performance of the system (silicon + package + PCB) and the electromagnetic interactions of each of the components of the system. Figure 7 below details the main steps involved. Firstly, the system’s physical design is designed with inputs from manufacturing/assembly rules and engineering/customer specs. Next, the electrical models of the package and PCB models for the high-speed channels are extracted using a full-wave 3D electromagnetic solver. The integrity of the solver has already been established in previous publications [6-8].

The extracted models are used in the next step of the flow, i.e., the system-level circuit analysis. In the system-level circuit analysis step, the S-parameters frequency domain models of the package and PCB are converted to time-domain coupled to the IO transistor spice netlist, and transient analysis is performed. The IO spice models are generated from a reduced-order model algorithm to speed up transient circuit analysis without impacting performance. The flow is exited if the requirements are met for the investigated figure of merits (i.e., insertion loss, return loss, crosstalk). If the conditions are not met, it is iteratively looped back to the silicon, package, and PCB physical re-designs until the requirements are met or exceeded.

Due to the complex process integration and the passive switch operational frequency, electromagnetic interactions at the system level (viz. silicon + package + PCB) are exacerbated. As such, optimal physical and electrical co-design techniques must be employed. The physical co-design involved the optimization of the device floor-planning, package, and PCB routing. Apart from physical design optimization for routability and manufacturability, it is critical to ensure that electrically there is no performance decay through the system transitions. Traditionally, electrical co-analysis approaches focused on each component's electromagnetic extractions separately and cascaded the models during the system-level analysis. Due to the high electromagnetic interactions at each transition, this approach cannot be applied to high-speed applications. Furthermore, the classical method of concatenating each model to represent the complete 3D behavior can lead to inaccurate modeling at an even lower frequency, as demonstrated in [9]. The validation of the integrity of the predictive signal integrity modeling methodology is discussed in the next section.

V. SIMULATION VS MEASUREMENTS CORRELATION

The packaged device was mounted on the evaluation module (EVM) PCB board shown in Figure 8 to evaluate the device's performance. The EVM board allows measurement of all eight channels simultaneously output for AC performance. The board has 8*3 = 24 high-speed pins; hence, high-density 8x1 Huber & Suhner connectors were used. This helped restrict the board traces’ length since the clearance area for separate connectors did not need to be accounted for. This also helped keep the area of the board relatively small.

For the highest accuracy in measurements, different calibration techniques are used to de-embed the losses due to the connector and differential traces path of the EVM board to accurately measure the actual silicon results. A high-frequency (vector network analyzer) was used to measure the complete system interconnect performance (i.e., DUT + cable + fixtures + traces). This ensures proper de-embedding to achieve highest measurement accuracy, the schemes below were employed (Fig. 9).
PLTS supports solving for Mixed Mode propagation → used to de-embed the differential traces
TRL provides accurate results at High Frequencies → Used to de-embed the cables, on-board connector, single-ended traces and AC-Coupling capacitors.

The AC performances were characterized over 17 devices to ensure a statistical representative sample in order to capture repeatability. Fig. 10 shows the measurements data acquired.

![Fig. 10. Measurements to simulation correlation (red showing meas.).](image-url)

Fig. 11 and Fig. 12 below shows the simulation to measurement correlations for both the insertion loss and return loss respectively.

VI. CONCLUSION

The signal integrity performance of a high-speed (20Gbps+) analog passive CMOS switch depends strongly on minimizing the electromagnetic interactions at the system level. This paper detailed the system-level signal integrity co-design modeling and silicon validation effort that led to the industry’s first high-performance, high-speed analog passive CMOS switch semiconductor device. The predictive modeling methodology allowed the assessment and quantification of the impact of the package-PCB interactions on high-speed signal integrity issues (i.e., insertion loss, return loss, and crosstalk). Direct laboratory measurements were performed on a 4-Channel 20 Gbps Differential 2:1/1:2 Mux/Demux IC designed on an evaluation module (EVM) to validate the predictive modeling methodology. Good correlations were observed between the simulation and empirical measurements. Implementation of the modeling methodology developed here should help, in the early design phase, to guide the design of future higher-speed analog passive CMOS switches.

REFERENCES


