A Precise Wafer Thinning Integration Process for nano-TSV Formation

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***Abstract*—This paper proposes the use of a Silicon-On-Insulator (SOI) substrate to control the final Si thickness on the substrate. After direct wafer-to-wafer bonding to another Si carrier wafer, a combination of grinding and etching is used to remove the Si substrate of the SOI wafer to expose the underlying BOX layer. Selective wet-etch process is then employed to remove the buried oxide (BOX) to stop on the thin SOI layer. Due to good wet etch selectivity between the BOX (oxide) and SOI Si, the remaining SOI Si thickness can be very well-controlled. In this paper, 175nm of remaining Si can be demonstrated on the bonded SOI wafer using this method. This method can be easily extended to even thinner final Si layers beyond 100nm. Nano-TSVs with dimension of 300nm diameter and 500nm depth are then fabricated on the thinned SOI which is bonded to another carrier wafer.**

Keywords—Wafer thinning, nano-TSV, Silicon-On-Wafer (SOI)

I. Introduction

Nano-TSVs are sub-micron Cu-filled vias, that can provide an option for efficient power delivery network through the backside of device wafers. The use of nano-TSVs helps to free up space on the wafer front-side [1], [2], [3]. In high-performance compute and AI hardware, nano-TSVs can also enable a significantly higher density of interconnects and thus increase data bandwidth between wafers that are directly bonded together. Another potential application of nano-TSV is in improving the efficiency of power delivery networks [4], [5]. While the formation of nano-scale TSV has already been widely established in CMOS back-end-of-line (BEOL) processes [6], [7], [8], the key challenge is to achieve thin Si thickness (<500nm) with repeatable, precise thickness control [9]. On the other hand, SOI substrates are being used as substrates on which various devices are built due to its resulting superior performance (e.g. low leakage, low power, higher switching speed) [10], [11], [12].

This work describes the use of a process flow to thin down a substrate wafer for nano-TSV formation. A 300mm SOI wafer is used to pre-define the final, required Si thickness after thinning. Finally, nano-TSVs are then fabricated on the thinned wafer to demonstrate integration feasibility.

II. Fabrication

A. Wafer Thinning Process

A SOI wafer with SOI Si thickness of 175nm on the buried oxide (BOX) is used. The buried oxide layer (BOX) is 2µm thick. Low temperature CVD oxide is first deposited on the SOI wafer before being bonded (via wafer-to-wafer fusion bonding) to another 300mm Si wafer, pre-deposited with oxide. Fig.1 CSAM image shows no delamination or air gaps observed post fusion bonding. Thereafter, edge trimming and mechanical grinding process are then performed to thin down the thick top Si substrate. An isotropic wet etching process is then performed to remove the remaining top Si substrate layer to expose the BOX layer. Subsequently, HF-nitric-acetic acid based etchant (HNA) and 100:1 DHF are used for removal of the BOX layer. It is determined that the wet etch selectivity of oxide to Si is 100:1, and etching can well-controlled to stop on the Si layer. Fig.2 illustrates in detail of the wafer thinning process flow. By using SOI wafers with the required SOI Si thickness, a precise, well-controlled and uniform thinning down process can be achieved.

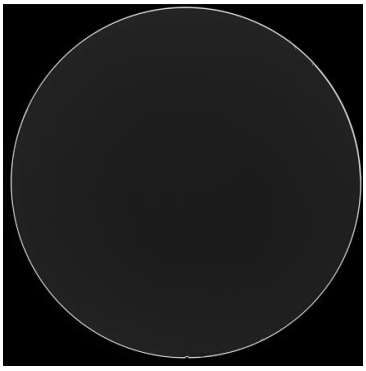

Fig 1. CSAM image post fusion bonding

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Thickness of the remaining BOX layer after HNA wet etch is measured using opti-probe technology and is as shown in Fig.3. Fig.4 shows the remaining Si layer after complete removal of the BOX layer (Both Fig.3 and Fig.4 show 49 measured points across wafer to center of the wafer). Comparison of the measured thickness in Fig. 3 and Fig.4 shows that any non-uniformity in the etching of the top substrate Si or BOX layer is non-critical and can be completely removed by the subsequent selective DHF etch process. A process challenge to note is the high wafer warpage of -377µm (Fig.5) observed after removal of the thick top Si substrate. This could be due to presence of the high stress BOX layer. This can limit the choice of process tools to remove subsequent BOX layer. Fig.6 shows the measured wafer warpage of -52µm after completely removal of the BOX layer. Upon removal of the BOX layer, wafer warpage is significantly reduced. This allows for subsequent processing in most tools.

Cross-section (XSEM) is performed at wafer centre and edge of the wafer after DHF wet etch. The XSEM image obtained is as given in Fig.7. XSEM analysis further verifies the thickness of remaining Si after the wet etch processes. A remaining Si thickness of ~0.17µm is observed at both XSEM samples taken from the wafer centre and edge. Through these results, it can be deduced that Si can be thinned down to any desired thickness as required.

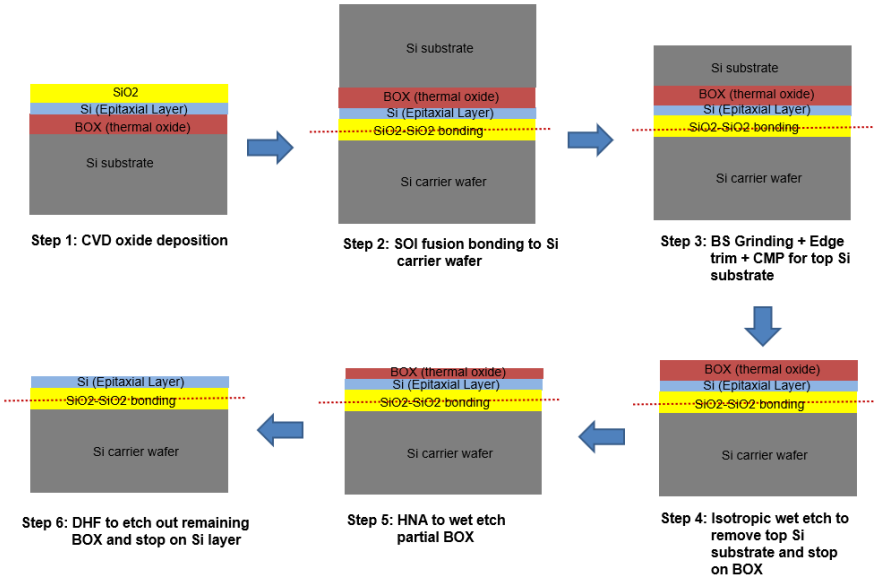

Fig 2. Wafer thinning process flow (The hatched red line indicates wafer-wafer fusion bonding interface between SOI and Si carrier wafers)

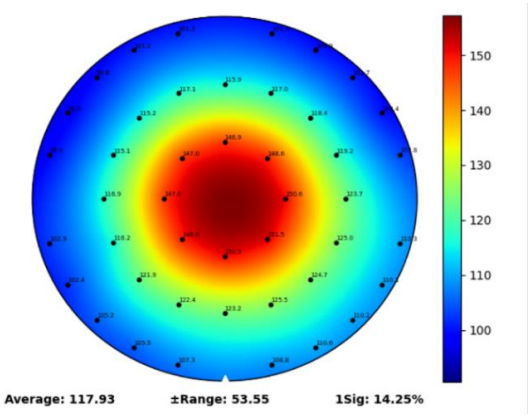

Fig 3. Remaining BOX thickness(nm) map post HNA etch

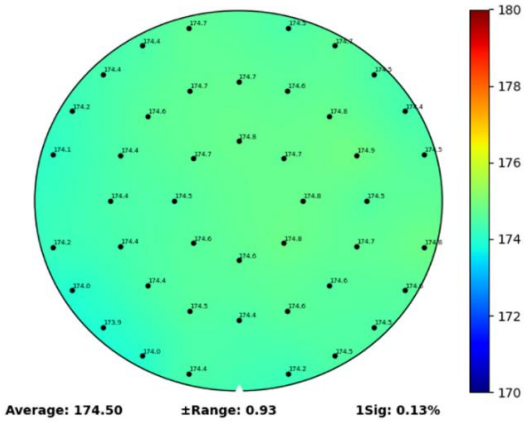

Fig 4. Remaining Si thickness(nm) map after complete removal of the BOX layer

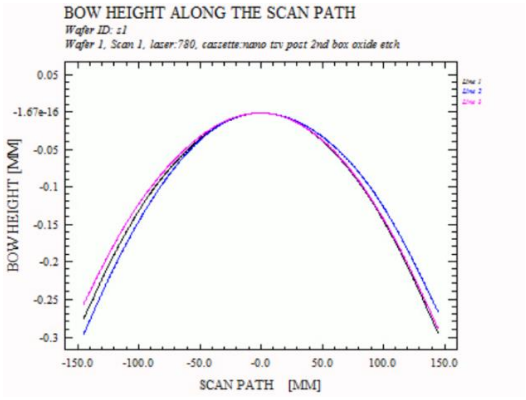

Fig 5. Wafer warpage post thick Si substrate removal

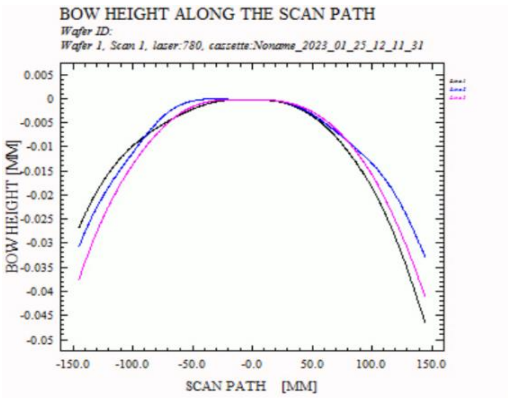

Fig 6. Wafer warpage post all BOX layer removal

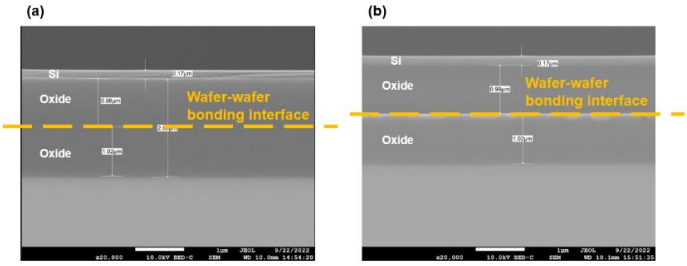

Fig 7. XSEM image shows final Si thickness of ~0.17µm for both (a) wafer edge and (b) wafer center after DHF wet etch. Yellow dotted line depicts the bonding interface between SOI and carrier wafer.

B. Nano-TSV Formation

Processed wafers which have undergone processes mentioned in Fig. 2 are then ready for nano-TSV patterning. A description of the nano-TSV process flow is shown in Fig.8. After thinning down of the SOI wafer by removal of the Si substrate and BOX layer, low temperature CVD oxide is deposited as backside passivation layer. Nano-TSV is then patterned on the Si layer using immersion lithography. Depending on the application and process needs, the etch process can be tuned to etch into the underlying oxide layer (for contact to potential embedded metallization) as shown in the TEM image of Fig.9(a). The etch process can also be controlled on the underlying oxide layer Fig .9(b). The void inside the nano-TSV is a sample preparation artifact caused by TEM filling material. An insulating dielectric layer Al_2O_3 of 5nm is deposited using Atomic Layer Deposition (ALD) process. TiN ALD is then used to fill the nano-TSV. No voids are observed after the nano-TSV is filled up with TiN as Fig. 10(a).

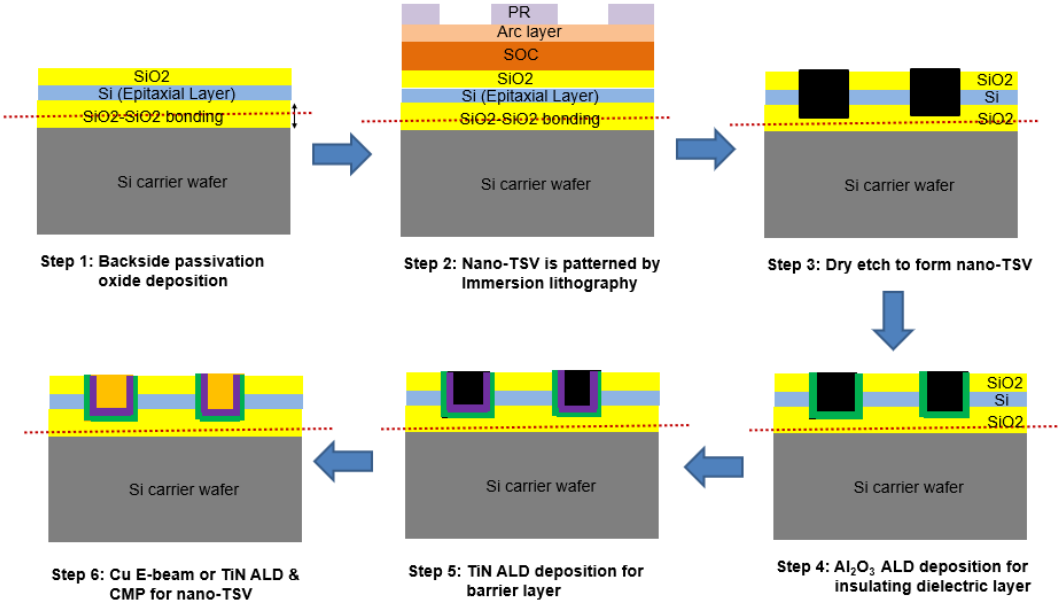

Fig 8. Nano-TSV process flow

Next, chemical mechanical polishing (CMP) is then done to remove the TiN overburden on the field region of the wafer. Fig.10(a) shows the TEM image of the nano-TSV after TiN CMP. ALD TiN shows good capability of gap filling and uniform deposition for the nano-TSV. It might provide void-free nano-TSVs for very small dimensions. However, TiN conductivity is relatively low and only around 17% of Cu. Therefore, it needs to apply other materials to fill up nano-TSVs (i.e., Cu, W, Ru, etc.) to increase conductivity. For Cu filling, a barrier layer TiN of 5nm is deposited using ALD again before performing Cu E-beam evaporation to fill the nano-TSV shown as Fig. 10(b). Cu-filled up TSV shows image contrast and EDX analysis on the field region of the wafer confirms the complete removal of the Cu overburden. A TEM image of the final nano-TSV structure on thinned, bonded wafer is given in Fig.11.

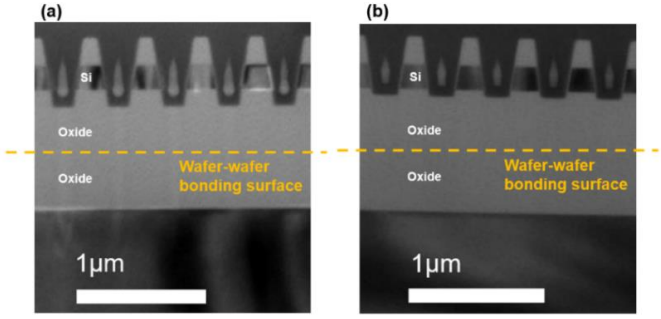

Fig 9. TEM image of nano-TSV after etching. (a) Etching into the underlying oxide layer; (b) Etching stop on the underlying oxide layer (The void inside the nano-TSV is a sample preparation artifact caused by TEM filling material)

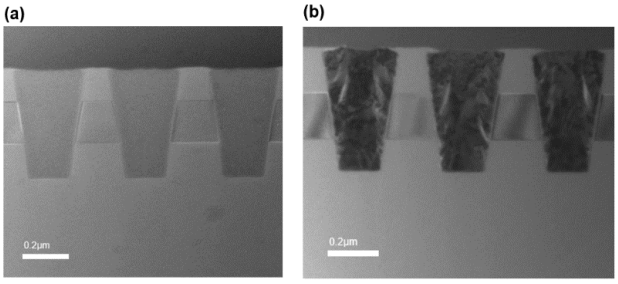

Fig 10. TEM image of nano-TSV after CMP (a) Nano-TSV filled up with TiN; (b) Nano-TSV filled up with Cu

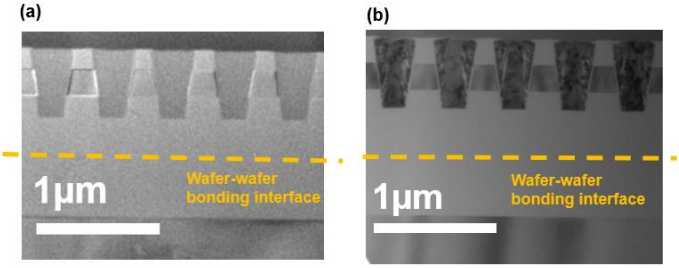

Fig 11. TEM image of the nano-TSV structure on thinned down, bonded wafer (a) Nano-TSV filled up with TiN; (b) Nano-TSV filled up with Cu

III. Conclusions

A precise, well-controlled wafer thinning process using SOI wafer is demonstrated. It can be induced that further thinner Si thickness beyond 100nm can be achieved by selection of the SOI wafers with a thinner Si layer. The fabrication of 300nm diameter nano-TSV is also demonstrated on the thinned bonded SOI wafer to verify integration feasibility. This provides possibility of application in high-performance computing and backside power delivery network.

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