Heterogeneous radio chiplet module for 5G millimeter wave application

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***Abstract*— While heterogeneously integrated packages for high performance computing have been presented, radio frequency (RF) applications have received less attention. In this work, we present an evaluation of a package for integrating two RF analog chiplets and a digital chiplet in a single high density fan-out package for 5G millimeter wave (mm-wave) applications.**

The two RF chiplets control antenna elements and the digital chiplet carries out the necessary signal processing. The chiplets were attached to a High-Density Fan-Out (HDFO) package with 2um/2um line width/space wiring designed for chiplet to chiplet communications. The HDFO was attached to a laminate, molded and a heat spreader (lid) was attached to realize a robust package.

The RF chiplet was designed in 22FDX® technology and was 3 x 16.5mm in size. The digital chiplet was designed in 12LP technology and was 4.5 x 16.5mm in size. The chiplets were thinned to 0.3mm and attached to High-Density Fan-Out with 25um diameter, 40um tall micro-pillar bumps. The chiplets were arranged with one RF chiplet on the North side, the digital chiplet in the center and the second RF chiplet, which was 180 degree rotated RF chiplet, on the South side. The gap between the chiplets was 70um. The chiplet to chiplet wiring was done with 2um wide traces that connected to 55um pitch micro-pillar bumps. The bump pitch was 55um at the edges of chiplets to facilitate a high density of wiring between the chiplets; elsewhere the bump pitch was 150um. The HDFO had four routing layers, front side pads for receiving micro-pillar and back side under bump metal for solder balls.

The HDFO was reflow attached to a laminate. The laminate had four metal layers for routing. Capacitors for power supply filtering were also attached to the laminate. This was molded and a 0.5mm thick, copper lid was attached to the top of the package to remove heat from the chiplets.

The thin RDL layers in the HDFO substrates presents design challenges for RF and mm-wave signal transfer and understanding these design challenges and the impact of them becomes important. The package therefore included several test structures to evaluate the performance impacts of different parts of the design stack, both in the package and the FC-CSP package.

The package was subjected to JEDEC stress tests to assess the reliability. Electrical readouts of daisy chains were acquired to monitor interconnect failure or degradation. Daisy chains were included in the FC-CSP laminate, HDFO, and at die level to test interconnects and reliability. Groups of daisy chains were used to differentiate between early failures and extended stress failures. The packages passed moisture level 3 pre-conditioning (40 parts) and unbiased highly accelerated tests (20 parts). The packages were assembled to PCB for Accelerated Temperature Cycling test (JESD22-A104 condition G)

Keywords—5G mobile communication, radio frequency, heterogeneous integration

I. INTRODUCTION

Heterogeneous packaging technologies enables high integration of chiplets. In a heterogeneous package different parts of the design can be designed as separate chiplets and connected via a variety of chip-to-chip interfaces. There are different motivations for building with chiplets - reuse for capacity scaling or reuse between product generations, mixing of process nodes for better performance, increase die process yield, lower power consumption or different vendors. It can also shorten the development cycle and lower the cost.

Different types of packages are available for chiplet designs like silicon interposer, silicon bridge solutions [5] and High-Density Fan-Out (HDFO) packages, [1-4] In the HDFO package the chiplet-to-chiplet connection is done in the redistribution layers (RDL) without any extra silicon. Most chiplet packages have been developed for digital designs. In this study we focus on an mmWave radio application. To be able to place the components on the backside of the antenna in a mmWave application the package size is important. The interface bump matrix is selected to have as small depth as possible.

II. METHODS

A. 22FDX® and 12LP chiplet design

Two test silicon dies were fabricated using the 2 top metal layers of the Back-End of Line (BEOL) in the process nodes 22FDX® (RF die) and 12LP+ (digital die). The aspect ratio for

2377-5726/23/$31.00 ©2023 IEEE
DOI 10.1109/ECTC51909.2023.00251

the RF die is 5.5:1 and for the digital die 3.7:1. On the RF die a sparse bump pattern is used for the RFIC mm-wave design. At the shoreline an 40TX/40RX AIB interface bump pattern is used for each RF tile. The bump pattern has a minimum pitch of 55 µm. On the digital die the matching AIB interface bumps are placed, and the rest of the area has a square pattern with 150µm pitch.

The 22FDX® technology is well suited for front end circuits due to the high fT/fmax properties of the technology node. However, 12LP+ has advantages in power and area scaling for digital circuits. With our partitioning of the chip architecture into 22FDX® and 12LP+, we were able to use the best technology node for the given functions, integrated in a single package.

B. High-Density Fan-Out design

The HDFO package used in this study is a chip-last type of package. The package included two RF chiplets and one digital chiplet. The package size is important for an antenna component in a mm-wave application. The HDFO package size is 18x12.6 mm, resulting in a package size only 24% larger than the total silicon area. Four RDL layers were used with a total thickness of 37µm. The ball pitch is selected to be 0.5 mm. The HDFO package is a molded package with exposed die, to ensure an efficient cooling. Figure 1 shows the schematic cross-section of the HDFO package while Figure 2 shows the top view of the fabricated components with all three chiplets visible.

Figure 1: Schematic cross section of the HDFO package

Figure 2: High density fan out module - Two 22FDX® analog chiplets (north and south) and one 12LP digital chiplet (center) are integrated in high density fan out.

The interface bump pattern selected for Die2Die interface testing is a slightly modified AIB pattern with 40TX /40 RX interconnects for each RF tile for each of the north and south dies. The AIB pattern is using the complete shoreline of the die. The bump pitch is minimum 55µm in the interface area and selected to 150µm in other areas. The bump pattern, package size and build up can be seen in Figure 3.

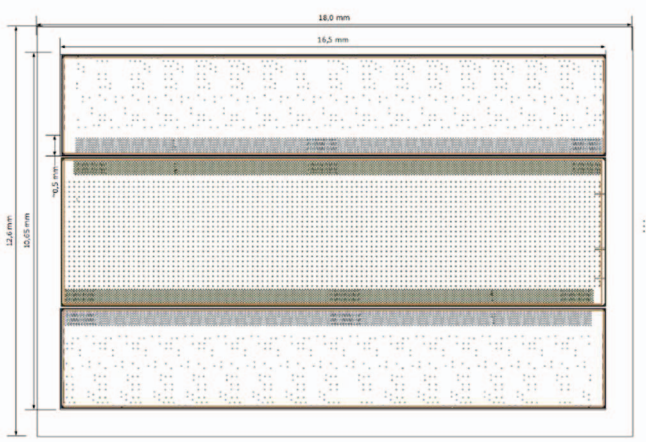

Figure 3: HDFO size and chiplet placement

According to the design, the 4 RDL layers are 3 µm thick and dielectric layer is 6 µm thick except for the last dielectric layer, passivation 5 in Figure 4, that is 13µm. This results in a 3µm distance between RDL layers.

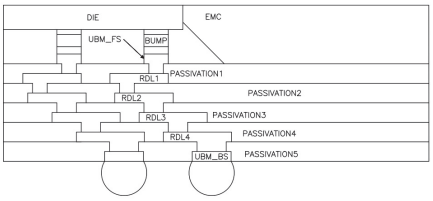

Figure 4: HDFO package layer stack up.

C. FC-CSP design

To enhance the reliability and the signal routing a Flip Chip-Chip Scale Package (FC-CSP) with a supporting laminate substrate was built. The substate was a 4-layer low CTE BT resin laminate suitable for high frequency RF packages. Decoupling capacitors were added on the substrate. The package is kept at the smallest possible size 24.1mmx18.6mm. A metal lid with a size of 16.6mm x 18.6mm and thickness of 0.5mm and a Thermal Interface Material (TIM) was included for good thermal conductivity. Solder balls are SAC 305 with a pitch of 0.5 mm. Figure 5 shows the schematic cross section of the FC-CSP package and Figure 6 shows the top and bottom view of the fabricated component.

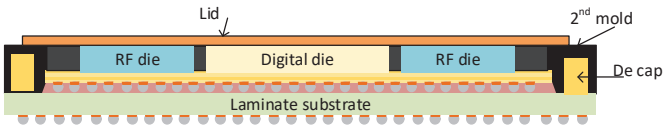

Figure 5: Schematic cross section for the FC-CSP, including the HDFO, decoupling capacitors, laminate substrate, a second mold and a lid.

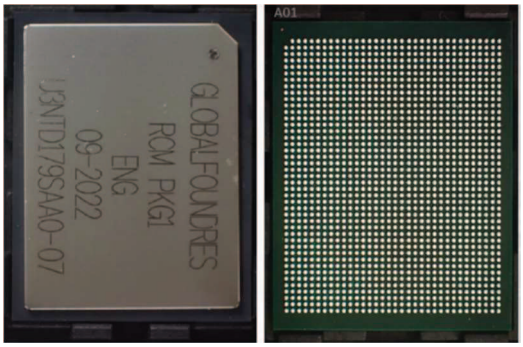

Figure 6: Packaged part - The top side with the lid is shown on the left. The BGA side is shown on the right.

D. *Daisy Chain test structures*

Two Daisy Chains were included in the HDFO design to monitor BLR of the assembled component. The two Daisy Chains were designed to differentiate between early failures (CC) and long-term deployment failures (DC) in solder joints in the HDFO to PCB interface. The CC Daisy Chain monitors a limited number of ball rows along the edge of the package, while the DC Daisy Chain monitors a large number (294) of solder joints in the center of the package. The test structures are depicted between RDL and laminate in Figure 7.

The additional substrate in the FC-CSP makes the previously described Daisy Chains available for reliability measurements between HDFO and the laminate. In addition, the FC-CSP includes additional test structures to monitor BLR of an PCB assembled package. As was the case for the HDFO there are two Daisy Chain available at the laminate-PCB interface, differentiating between early failures (CC) and long-term deployment failures (DC). The CC Daisy Chain monitors the edge rows of solder joints, while the DC Daisy Chain monitors the center solder joints (668 solder joints for the FC-CSP). The test structures are depicted between laminate and PCB in Figure 7.

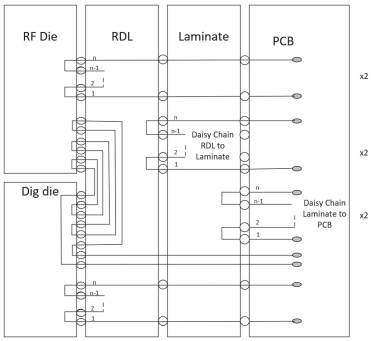

Figure 7: Daisy-Chain structures included in the design on different levels.

E. *WIO die2die interface*

The bump depth of the AIB interface used between the chiplets was a maximum 7 bump rows, out of which 2 rows was used for power and ground and the remaining 5 for signals, as shown in Figure 8 for an enlargement of the fan-out region of 2 AIB columns from the RFIC.

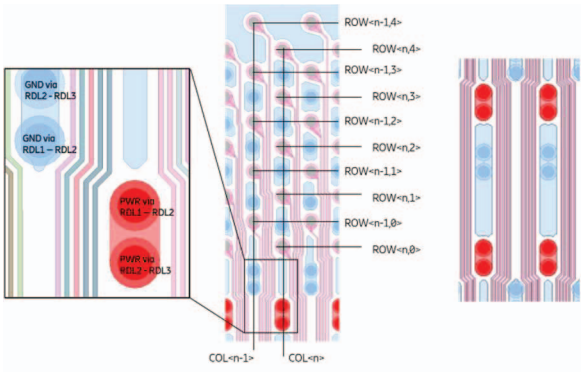

Figure 8: AIB fan-out for 2 columns and 5 rows

The narrow path in between the vias for the ground and I/O supply are the limiting factor for being able to fit all the 5 signal rows on one single layer. However, with the 2µm line width and space (L/S) all 5 signals per column fit, thus enabling routing of the full 40TX/40RX interface for one tile occupying 1mm shoreline width. All signals were routed on RDL2 in the HDFO stack-up using a strip-line configuration as shown in Figure 9, in which RDL1 and RDL3 were assigned to ground acting as reference planes for the strip-line.

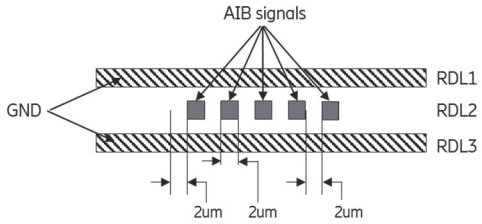

Figure 9: AIB die-to-die routing topology

To assess the signal integrity of the dense signal routing of the AIB interface a simulation model has been developed in Ansys High-Frequency Simulation Software (HFSS). The ports for the simulation are assigned between the signal and ground reference on the IC-pad for each die, respectively. Thus, the Cu-pillar and solder bump transitions in the underfill region between the IC and RDL are included in the model. The motivation for doing this is that the coupling in between the tightly spaced signal bumps likely is a contributor to the coupling between the signals and thus will impact the signal integrity. In Figure 10(a) a cross section view of the manufactured HDFO can be seen. Figure 10(b) shows a detailed cross section of the µ-bump area of the finished HDFO package and Figure 10(c) shows the corresponding cross section of the simulation model, where the location of the ports for the SI-model is indicated.

A subset of the AIB signals were simulated, representing a 10-signal group routed in between the coplanar ground planes in Figure 11. The selected signals contain 4 signals assumed driven from RF IC (RF_TX/DIG_RX), 4 signals assumed driven from the digital IC (DIG_TX/RF_RX), and a differential clock pair, which in the simulation is assumed driven from the digital IC. Figure 11 shows the signal mapping on the signals included in the simulation model.

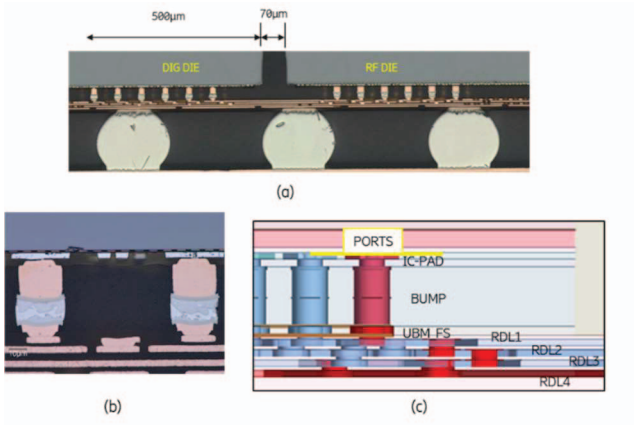

Figure 10: (a) Cross section of AIB simulation model with RF & Digital IC mounted on the HDFO RDL. (b) Cross section of the µ-bump area between the IC and HDFO. (c) Cross section of EM model.

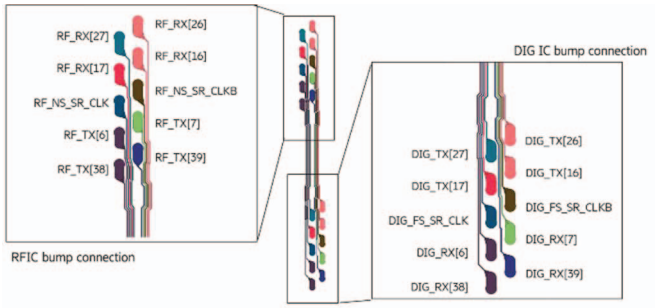

Figure 11: Signal mapping of the AIB signals in the EM simulation model

F. RF test structures

To evaluate designing mm-wave design in the thin RDL of the HDFO package, different passive test structures have been included in the package design. One of the structures was a shorted half-wavelength resonator. Tuning the resonance frequency was done by changing the length of the shorted stub, and a total length of 2mm was chosen, which for the stack-up and dielectric material parameters, given at the time of the design, resulted in a resonance frequency of around 42GHz.

Figure 12 shows the implementation of three RDL2 transmission line routing structures. All transmission lines were implemented as strip-lines with ground reference on both RDL1 and RDL3. This results in that the RF signal can be shielded well inside the HDFO stack-up, thus limiting undesirable coupling.

As the vertical stack-up and distance between signal and ground reference is small (3um) the signal trace width needs to be rather thin as well to reach a line impedance of around 45Ω. For the RDL2 traces a line width of 3um was used. A simulation of the loss of only the RDL2 strip-lines indicates a loss of 0.65dB/mm for the chosen strip-line topology. Two of the transmission lines have been implemented in such a way that they are routed with 6um spacing between the lines for around 3mm without any ground shielding in between. This was intentionally done to enable analysis of the line-to-line crosstalk.

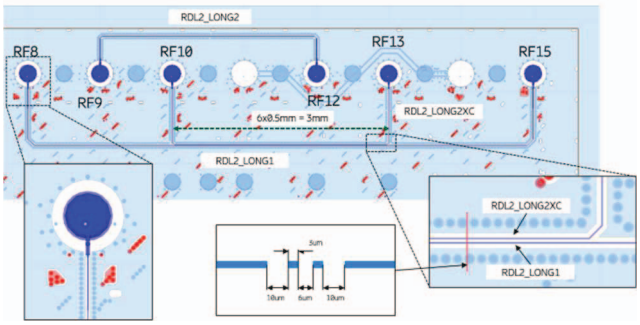

Figure 12: Design detail of the HDFO implementation of long RDL2 transmission line structures

One of the challenges found when routing mm-wave signals in the thin RDL stack-up of the HDFO was to handle the large parasitic capacitance introduced by the large solder-ball pad on RDL4 and the close proximity to the ground plane on RDL3 and upward. This capacitance creates a very low impedance in the solder ball transition which becomes difficult to match to the transmission line impedance. The mitigation to this was to open up RDL layers above the solder ball pad for all layers

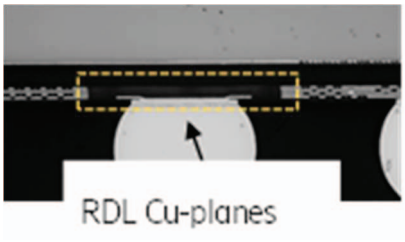

Figure 13: Cross section of the HDFO to FC CSP solder ball interface for one of the RF signals.

This however means that the mm-wave signals will not be contained within the HDFO stack-up but can radiate out or pick up radiation externally. If the signal pad is under the die this means that the signal pad can couple to the structures in the die. If the signal pad is instead outside the die area the RF signal will radiate into the mold, risking to interfere with other exposed signals. Both challenges need to be analyzed or in worst case be mitigated by various shielding structures without adding excessive capacitance.

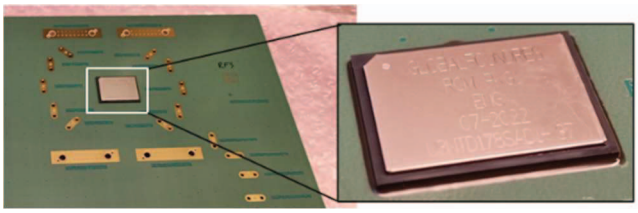

Figure 14: Package mounted on the RF test PCB

The package was mounted on a designated RF PCB to enable measurements on the test structures described above. High frequency RF connectors were used to connect to the PCB and a calibration kit was used to de-embed into the PCB to a common reference plane for all structures. Figure 14 shows the RF test PCB with the package mounted.

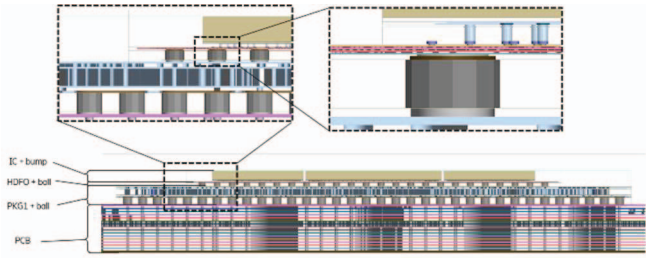

Figure 15: 3D EM model for simulation of RF test structures.

A simulation model has been developed in Ansys HFSS of the final component implementations. This model included PCB, FC-CSP, HDFO, and ICs with detailed models of all device-to-device transitions, such as µ-bump, C4 balls, etc. as shown in Figure 15. FEM simulation of the RF structures was run with the simulation model cut so that the same reference plane was used in the simulation as for the de-embedding point of the measurements. This enabled comparisons and correlations of the simulation models to measurements.

G. Reliability Test Plan

1) MSL3 and uHAST

The component level reliability was assessed following JEDEC standards. The following stress tests were applied to the parts:

a) Moisture sensitivity level 3 (MLS3)- preconditioning.
40 parts were baked at 125°C for 24 hours, soaked at 30°C temperature and 60% relative humidity for 192 hours and reflowed (3x) at 250°C peak reflow temperature

b) Unbiased highly accelerated stress test (20 parts).
20 MSL3 pre-conditioned parts were placed at 110°C temperature, 85% relative humidity and 17.7 psia pressure for 264 hours.

At the end of the stress tests, the parts were assessed by electrical readings and Confocal Scanning Acoustic Microscopy (CSAM) imaging.
The electrical readouts from daisy chains were analyzed for open circuits that would indicate a failure or a higher than +/-20% change in resistance that would indicate a degradation of the interconnects. The CSAM images were reviewed for any cracks or delamination in the package.

2) Board level reliablity,Temperature cycling

The packages were tested for Board level Reliability Temperature Cycling (TC) according to JESD22-A104 condition G (-40°C to 125°C). The sample size was 32 HDFO and 32 FC-CSP in total. The resistance was measured on all Daisy Chains before the test and the main chains described above in section D were monitored by an event detector during test. The modules were divided into subgroups with and without underfill.

H. Fabrication and Assembly

1) Package

The high-density fan-out (HDFO) layers were constructed on a 300mm carrier wafer first. The 22FDX® and 12LP wafers were bumped (25um diameter, 40um height copper pillar), diced and chiplets were reflow attached to the HDFO wafer. This was followed by capillary underfill and mold. The wafers were thinned for a final thickness of 300um for the chiplets and flipped and solder balls were attached. The individual HDFO packages were then diced.

The HDFO packages were attached to FC-CSP in a standard panel level assembly process. The steps included reflow attaching the HDFO to the laminate, underfill and molding. The mold was thinned to expose the backside of the chiplets and a heat spreader (0.5mm thick copper) was attached using thermally conductive epoxy. As a final step, solder balls were attached to the laminate and diced to realize unit level packages.

2) Board assembly

Both HDFO and FC-CSP packages were assembled, using reflow soldering, to a 16-layer µvia Daisy Chain test board with a total thickness of 1.6 mm. The assembled components were checked in X-ray and all solder joints passed Ericsson's acceptance criteria.

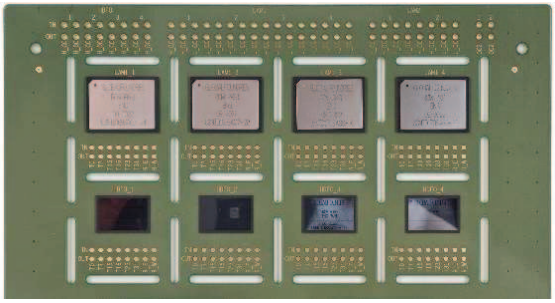
Figure 16: HDFO and FC-CSP packages mounted on daisy-chain PCB.

I. Construction analysis

The package was placed in potting material, cut and polished for cross sectional analysis. The thickness of metal layers, dielectric layers and component heights were measured. The results were compared to design targets. A cross section of the finalized FC-CSP assembly with HDFO and chiplets are shown in Figure 17.


Figure 17: Cross section view of the assembled package

J. Co-planarity characterization

Warpage characterization was done on both the HDFO and the FC-CSP package using Shadow Moire technique. Using Instrument TherMoireAXP.10 parts were baked at 125°C for 24 hours. 5 parts were selected for 'dry' measurement and 5 parts were 'moisture soaked' (168 hours in 85°C & 85% relative humidity). All components were shown to fall within the warpage requirements as defined by the JEDEC 'Standard Practiced and Procedures SPP-024A' which allows for +150/-100 um from flux activation (150°C) to peak reflow temperature (250°C).

III. RESULTS

A. Build assessment

The data from the construction analysis are given in Table 1 and Table 2. As given in the Table 1, all parameters were within 12% of the expected values.

Table 1: Summary of construction analysis

Parameter	Expected (um)	Measured (um)	Variation (%)
Heat spreader thickness	500	496	0.8%
Die 1 thickness	300	298	0.7%
Die 2 thickness	300	300	0.0%
Die 3 thickness	300	299	0.3%
HDFO thickness	44	39	11.4%
Capacitor height	200	221	10.5%
Laminate thickness	386	382	1.0%
Package thickness	1747	1621	7.2%

The high-density fan-out layer thicknesses are given in the following Table 2. As shown in the table, the copper layer thickness was within 10% of the expected value and the wiring width was within 5% of the expected value.

Table 2: Summary of RDL cross-section measurements

Parameter	Expected (um)	Measured (um)	Variation (%)
RDL1	3	3.2	6.7%
RDL2	3	3.3	10.0%
RDL3	3	3.2	6.7%
RDL4	3	3.3	10.0%
Width of traces (RDL2)	2	1.9	5.0%
Spacing (RDL2)	2	2	0.0%

B. Simulation on WIO die2die interface

Figure 18 shows the transfer characteristics for the die-to-die AIB interface, for an average routing length of between the dies around 750um. Signals that have multiple adjacent neighbors have slightly larger loss, while signals on the edges behave better. This is also more pronounced at above 10GHz for which signals with multiple adjacent neighbors drop off faster.

Figure 19 shows the far-end crosstalk simulation results for the receiver RF_RX17 (at RFIC bump). In the figure the corresponding eye-diagram is also shown for a PRBS pattern at a data rate of 32Gbps. The single ended crosstalk from CLKB to RF_RX17 contributes to both voltage and timing noise that closes eye opening. However, the signal integrity in this scenario shows that the 2 Gbps data-rate for the AIB interface is achieved with large margin, and it should be feasible to push the bit-rate quite a bit higher.

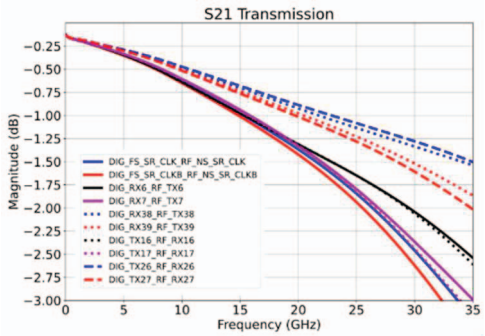

Figure 18: Insertion loss (IL) AIB signals (bump-to-bump)

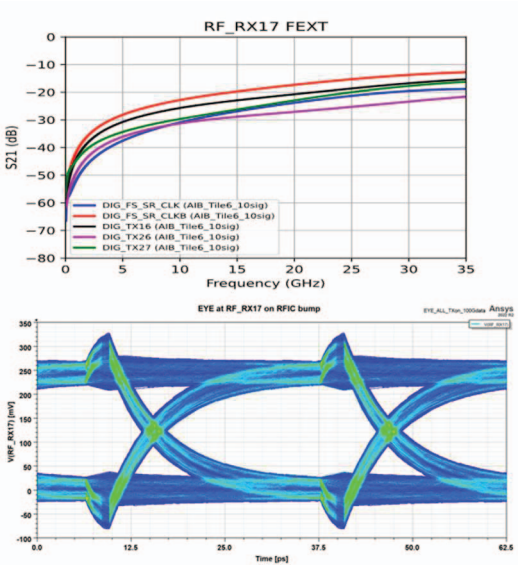

Figure 19: Crosstalk and EYE diagram at RF_RX17 receiver bumps of a 32Gbps signal, Zo=50ohm.

C. RF measurements and simulations results

1) Resonator results

Figure 20 shows the simulation and measurement results for the shorted stub resonator on RDL2. Figure 20(a) shows the measurements versus the original simulation model. The simulation model matches measurements to a very high degree, but as can be seen the frequency of the resonance is shifted roughly 1.5GHz down to around 40GHz for the measurements compared to the simulation.

The cross-section analysis of the HDFO stack-up HDFO shown in Table 2 gave that the thickness of the copper traces in the produced component was larger than in the stack-up used in the original simulation model. Hence, an updated simulation model was developed considering the thickness increase. The total stack-up height was kept, meaning that the dielectric gap in between the signal and ground planes for the RDL2 strip-line was reduced, which impacts the effective dielectric constant and hence the resonance frequency. In Figure 20(b) the simulation results using the updated HDFO stack-up model can be seen. The resonance in the simulation and measurements are now matching better.

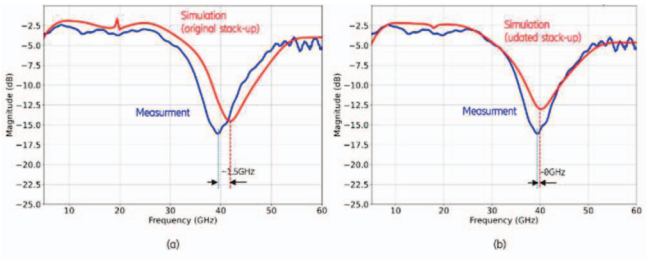

Figure 20: S21 magnitude results for RDL2 resonator on HDFO mounted on PCB - measurements vs. simulation model
(a) simulation with original HDFO stack-up model
(b) simulation with updated HDFO stack-up model

2) Transmission line loss results

Figure 21 shows the simulation and measurement results for the RDL2 transmission lines. The developed EM simulation model is accurately describing the measured data. Figure 21 also includes the loss in the transition from the evaluation PCB up through the HDFO stack to the RDL2 routing layer. To calculate the loss/mm the delta between each of the three lengths are calculated as shown for 4 frequency points in the table in Figure 21. Comparing the average loss per millimeter between measurement and simulation shows that the results are matching rather well, indicating a loss of 0.75dB/mm and 0.87dB/mm for 28GHz and 37GHz, respectively.

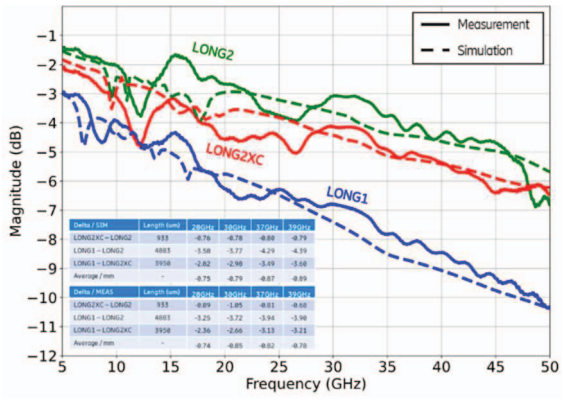

Figure 21: Simulated and measured S_{21} results for RDL2 traces in the HDFO stack with 4 different lengths

Figure 22 shows simulation results for two ideal microstrip transmission lines in the FC-CSP laminate substrate in Figure 5. This result would indicate that the loss per mm in the RDL transmission line was around 8-9x higher than routing on a normal package laminate. However, the FC1 lines in Figure 22 are routed in a 4-layer substrate where only microstrip transmission line configuration was possible. An advantage is that this enables use of wider lines and still reach 50 ohm impedance, but on the other hand makes it difficult to shield properly due to that the signal is exposed. Especially if the lines are routed at the layer facing the core layer due to the larger core-vias. In a more RF optimized FC-CSP laminate stack-up, enabling shielded strip-lines, the closer distance between signal and ground planes would reduce the RF trace line width to around half for a 50 ohm line, thus increasing the transmission loss by roughly 2x.

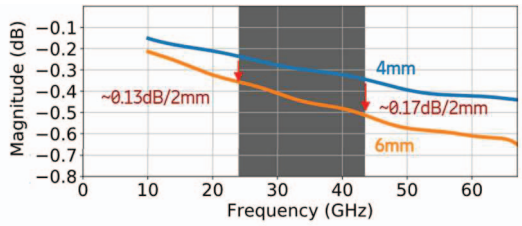

Figure 22: Simulation results for a transmission line on the package laminate stack-up

Further, adding the larger effect of surface roughness and larger edging effects in FC-CSP package laminates compared to the HDFO stack-up [1] would further increase the loss of the RF lines in the package laminate. A reasonable increase of loss compared to the ideal case would be in the range of 1.5-2x. Hence, taking all this into account the loss penalty of routing mm-wave signals on thin RDL lines is estimated to be 2-3x compared to routing in the FC-CSP laminate when using the same line impedance. Thus, for shorter distances it is possible to route mm-wave signals in the RDLs, and the fine design rules enable very good shielding possibilities. However, longer fan-outs especially at frequencies above 40GHz should be done outside the HDFO.

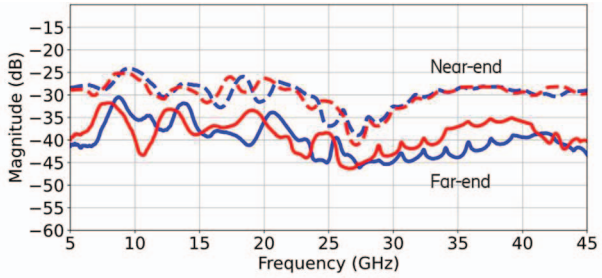

Figure 23: Measured crosstalk between RDL2 traces on two boards (red PCB1, blue PCB2). Dashed curves NEXT and solid FEXT

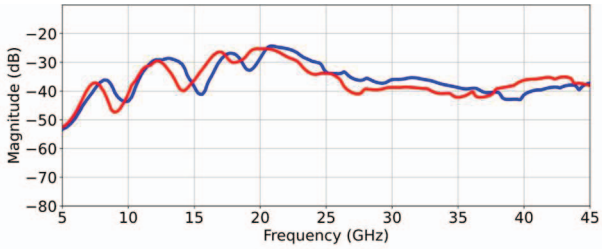

Figure 24: Measured adjacent ball coupling on the HDFO

3) Crosstalk results

Figure 23 shows the crosstalk measurements on two RF PCBs between the two adjacent RDL2 traces for both the Near-end crosstalk (NEXT) and the Far-end crosstalk (FEXT). According to the results the NEXT (dashed in Figure 23) is around -25dBc for the frequency range of 5-20GHz. In this area the matching of the structure is not as good, which means that more of the aggressor signal will reflect back to the victim, due to mismatches in ball transition. In the frequency range where the matching is better (25-40GHz) the crosstalk is reduced to

around -30 to -35dBc. The FEXT is generally around 5-10dB lower than the NEXT.

Figure 24 shows the measured ball-to-ball coupling between the HDFO and the PCB for 2 different PCBs. The ball-to-ball coupling is peaking at -25dBc at the frequency of 20-25GHz. In this frequency range the test structures were slightly un-matched, resulting in reflections at the far end possibly increasing the crosstalk. In the frequency range where the structure was designed for (30-40GHz) the matching for the simulation is good and here the coupling drops to -34dBc to - 40dBc. The single row GSGSG ball pattern of the HDFO shown in Figure 24 and the HDFO stack-up routing results in around -35dB isolation frequencies up to 30-35GHz provided that good matching is obtained.

D. Package reliability

All 40 parts passed the moisture sensitivity level 3 (MSL3) test. There were no open/short circuits in the electrical data. The readings were within +/- 20% compared to pre-test readings. There were no abnormalities in the CSAM images.

All 20 parts passed the unbiased highly accelerated stress test (uHAST). The electrical readings were within +/- 20% of the pre-test data. There were no abnormalities in the CSAM images.

E. Board level reliability

Test boards populated with HDFO and FC-CSP components, 32 samples of HDFO (20 with UF) and 32 samples of FC-CSP packages (12 with UF), were run through TC, 1000 cycles at –40°C to 125°C at a cycle time of 52 min. The component and PCB Daisy Chain (CC & DC) resistance were continuously monitored using an event detector. UF (Henkel Loctite Eccobond UF 1173) was used to increase the reliability of the assembled packages. After TC a 100% pass rate (0 failures) could be observed for components with UF. The FC-CSP package was put through additional TC, still with a 100% pass after 2000 cycles. The characteristic failure rate of components without UF was 40 cycles for the HDFO and 348 cycles for the FC-CSP package. The solder joint fatigue was seen to propagate from the package edge towards the center of the board assembled packages.

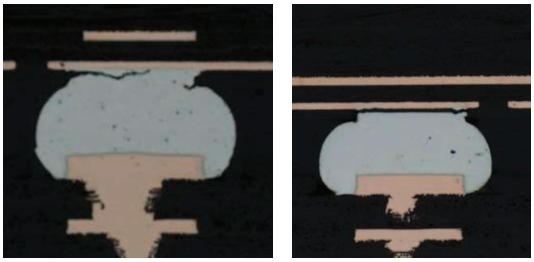

Figure 25: To the left, Cross section of FC-CSP package DC chain. Cross section after 579 cycles. To the right a crack in the IMC in CC. Cross section after 1000 cycles.

A dye-and-pry analysis showed that typical failure mode is a fracture on the components side. The failure modes found was either a fracture in the intermetallic compound (IMC) interface or in the bulk solder on the component (see Figure 25).

IV. DISCUSSION

We have demonstrated heterogeneous integration of three chiplets (2 analog RF chiplets and 1 digital chiplet) using High-Density Fan-Out package. This heterogeneous integration enables the partition of the beamformer circuits to an implementation that matches the circuit functions to the most suitable technology node (22FDX® for analog and 12LP for digital).

The HDFO package was designed for chiplet-to-chiplet communication using the Advanced Interface Bus (AIB) protocol. Simulations showed the wiring between the chiplets were capable of 2Gb/s per wire data transmission.

RF test structure design and measurements show that it is possible to do mm-wave design in the thin stack-up of the HDFO. However, care must be taken on limiting the routing distance due to the excessive loss of the thin lines and proper model need to be developed accounting for parasitic effects in bump and C4 ball pad regions.

The construction analysis showed package dimensions closely matched to expected design targets. In component level reliability tests, the parts passed the moisture level 3 and unbiased highly accelerated stress test.

The Board Level Reliability testing showed that underfill will be needed for both the HDFO package and the FC-CSP package to fulfill the Temperature Cycling requirement.

ACKNOWLEDGMENT

This project was a co-development between Ericsson and Globalfoundries. The authors thank Ericsson's Anne-Kathrine Knoph, Benny Gustafson, and Peter Svensson and Globalfoundries Kashi Vishwanath Machani, Frank Kuechenmeister, Yunyao Jian and Scott Pozder for all the technical support. The contributions from the following organizations are also acknowledged: Centre de Collaboration MiQro Innovation (C2MI), Bromont, Canada and Amkor Technology, Tempe, Arizona.

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