Abstract—This paper presents novel technology developments for vacuum wafer level packaging of microbolometer arrays for thermal infrared sensors targeting applications in automotive, safety, and security/surveillance. The concept is based on fabrication of large cap structures on temporary carrier wafers and their subsequent transfer bonding to device wafers. The objective of the presented work was to develop and test wafer level vacuum packaging for MEMS microbolometer arrays (MBA) fabricated on read out integrated circuit (ROIC) wafers. For that, related MBA layouts integrating diverse Pirani vacuum test structures were fabricated on 200-mm silicon wafers.

With intent of hermeticity, all wafer bonding steps were done by AuSn soldering using seal rings, which were deposited by electroplating. The relevant process flows with alternative process options as well as the obtained results of the capping approaches are presented and discussed extensively in this article.

For characterization of the sealing results, Pirani test structures were utilized. First, their resistance vs. pressure behavior was determined under controlled reference vacuum. The measured resistance values of identical structures after capping were then compared with the reference data to estimate the residual vacuum inside the cavity of the bonded cap structures.

Keywords—wafer level packaging, wafer level capping, hermetic sealing, vacuum packaging, MEMS packaging, microbolometers, Pirani sensors, permanent wafer bonding, temporary wafer bonding

I. INTRODUCTION

Visible light cameras enable the recording of images of properly illuminated objects using electromagnetic waves in the range from 0.4 to about 0.7 μm. Imaging at wavelengths beyond 0.7 μm is very useful because it reveals additional information about the objects and enables new applications. However, imaging at longer wavelengths requires cameras with special infrared image sensors and different optics [1, 2, 3]. Among the many types of infrared image sensors and detector technologies, there are microbolometers, which have enabled uncooled and thereby affordable thermal infrared cameras. Such thermal infrared cameras allow one to acquire images from objects by their radiated heat, that is, by the emission of infrared radiation as described by Planck’s radiation law. Microbolometers are mostly sensitive to long-wave infrared (LWIR) (8-14) μm, which coincides with the transparent band in the earth atmosphere. Like visible light cameras, the thermal infrared cameras have many applications and large markets in defense, transportation, surveillance, firefighting, thermography and outdoors leisure. Many new application areas are enabled by
reducing the cost and further improving the performance and reliability. The latter are greatly influenced by the microbolometer packaging, that is, the cap covering the microbolometer array, the vacuum level under the cap, and any change of vacuum level over time. Finally, packaging microbolometer arrays at wafer level can reduce the cost compared to chip or device level packaging.

The here presented wafer level capping approaches involve cap structures that were transfer-bonded simultaneously from a donor wafer to a receiver wafer (i.e. device / ROIC wafer). The cap structures were fabricated from silicon wafers, with high infrared (IR) transmission in the LWIR range, which were temporary mounted on carrier wafers. For the wafer level fabrication of the caps and in the scope of wafer transfer bonding, they were adjusted in size to the MBA arrays as well as created with mirrored layout to their locations on the receiver wafer. This enabled partial capping of the receiver dies by wafer bonding techniques and allowed post bond access to peripheral areas of the dies with input-output (IO) pads.

In this work, two fabrication approaches for cap structures were tested, which can enclose large volumes. In the first approach, monolithic caps with a deep cavity were created by deep reactive ion etching (DRIE) from standard silicon wafers. In the second approach, hybrid caps of enlarged volume were created by bonding silicon frames to flat silicon or germanium lids, which were also both prepared on temporary carrier wafers. The carrier from the frame side was then removed first to enable subsequent bonding of the hybrid caps to the MEMS device / ROIC wafer.

Microbolometers are microelectromechanical systems (MEMS) with a freestanding and thereby thermally isolated membrane, which can absorb infrared radiation and converts the absorbed energy into heat. [4, 5] The temperature change of the microbolometer membrane causes a change of the electrical resistance, that can be measured by a readout integrated circuit (ROIC) fabricated in complementary metal-oxide semiconductor (CMOS) technology. According to the thermal principle, microbolometers have to operate in vacuum to reduce thermal loss from convection. Therefore, a cap has to be applied onto the microbolometers which provides vacuum and a hermetic sealing towards the surrounding air. The cap has to be transparent in the LWIR to enable a maximized incident radiation onto the microbolometers. The herein fabricated microbolometers feature a pixel pitch of 17 μm and are arranged in an array of 640 x 480 pixels (VGA resolution). The entire pixel array has to be reliably sealed in vacuum over life time by the provided cap. Due to the VGA resolution as well as the requirement to enclose additional die area for getter deposition, relatively large caps with lateral dimensions of 12.3 x 11.2 mm² have to be used here. The microbolometer die itself including all peripheral circuitry and IO pads has a size of 13.6 x 13.1 mm². With this geometry, all IO pads of the microbolometer die will be accessible with distance between edge of the cap and IO pads in the range of 350-500 μm.

Microbolometer processing requires compatibility with post-CMOS integration, including a temperature limitation of around −450 °C in all manufacturing steps. Based on that, also the applied wafer level vacuum packaging processes have to be compatible with this temperature restriction.

The microbolometers were fabricated at 200 mm scale on a test ROIC with only top metal layer. ROIC/MEMS interface were prepared by opening the top passivation of the ROIC wafer and filling the vias for contacting MEMS and ROIC. Microbolometers were fabricated in a microsystem’s technology with use of a sacrificial layer, which supports and protects the bolometers during the fabrication and which is removed finally to create the sensitive MEMS structures. Figure 1 demonstrates freestanding microbolometers on top of the designed test ROIC after removing the sacrificial layer. An array arrangement of microbolometer pixels with 17 μm pitch consisting of a sensor membrane with lateral legs can be seen.

In order to enable the wafer level capping process, a deposition of solder frames is required along the outlines of the micro bolometer arrays. In order to enable this, the sacrificial layer was first removed in the locations were the solder has to be deposited. The solder frames were prepared by electroplating and finally the sacrificial layer was removed. It had to be ensured with several experiments, if the removal of the sacrificial layer works after the solder was deposited and if the removal process somehow damages the solder or causes insufficient solderability.

![Figure 1: SEM image of microbolometer pixels with 17 μm pitch](image-url)

This microbolometer array also contains alternative sensor layouts, which can be evaluated as micro-Pirani elements. [6, 7] Different types of micro Pirani elements were designed and manufactured to evaluate the vacuum pressure inside the package. Pirani test arrays comprising different sensor types by changing the thermal isolation and resistance of microbolometer membrane. These micro Piranis use the same post-CMOS processing like the microbolometers and therefore do not increase the production cost while adding an important feature
to the product. The possibility to monitor the vacuum pressure using micro-Pirani sensors is still under investigation. The micro-Pirani sensors have same dimensions and structure as the microbolometer pixels. The reflector layer on the Si substrate of the microbolometer pixel acts as the heat sink for the designed micro-Pirani sensors.

III. OPTIONS FOR PREPARATION OF DONOR WAFERS WITH CAP STRUCTURES

The usage of donor wafers for preparation of cap structures and their subsequent transfer bonding to device wafers is one core approach of wafer level capping technologies. [8] The cap structures are fixed in face up direction on the donor wafers and can be released from those after completion of the transfer bonding step. The positions of the cap structures on the donor wafers are matching with the die pattern on the receiver wafer. The caps on the donor wafers can be either created from processing of a former bonded wafer or they can also be placed onto the donor wafers. Both options enable, that the lateral dimension of the caps can be smaller than the dimensions of the receiver dies. This so-called “partial capping” allows that peripheral areas on the receiver dies such as IO pads can still be accessed after the caps are bonded.

The following three sections describe in detail three different options for the preparation of donor wafers with cap structures specifically adequate for encapsulation of large volumes required for vacuum packaging of former presented microbolometer arrays. All capping approaches in this work are based on AuSn soldering using seal rings of Au+Sn and Au, which are pre-deposited on device wafer and cap donor wafer side respectively. Furthermore, in all approaches B33 glass wafers with 200 mm diameter and 500 μm thickness are used as carrier wafers. For temporary bonding purposes a thermoplastic adhesive material is used. The material allows the final detach of the glass from the cap structures after bonding by laser assisted de-bonding using a 248 nm excimer laser stepper.

A. Fabrication of Monolithic Silicon Caps

With the given boundary conditions of maximizing the encapsulation volume in a same time of compact size (die per wafer, access to IO padring), the generation of cap structures by recess plasma etching in thick silicon wafers seems to be the most logical and practical way. The process flow in Figure 2 shows how donor wafers with monolithic silicon cap structures having plasma etched recess and deposited metal ring for later soldering can be prepared. As starting material silicon wafers with optical grade / high infra-red transmission capability and thickness of 650 μm as well as 500 μm thick glass wafers are used, which is shown in picture 1. As first steps, an anti-reflective coating (ARC) is deposited on the front side of the silicon wafer (green layer in picture 2). The glass wafer is sputtered with a thin metal layer, which is structured by wet etching. This metal layer (indicated in blue in picture 2) will later block the laser during the de-bonding step for selective debonding. This enables, that only the cap structures will be released from the donor wafers whereas surrounding areas remain on them. Following, the temporary adhesive layer (yellow) is coated on the carrier wafer to enable a subsequent adhesive wafer bonding of silicon to carrier wafer, which is shown in step 3 of Figure 2. In the next step, the silicon wafer is polished on the back side, a thin silicon oxide is deposited and the Au seal rings are deposited by semi-additive technology (step 4). Semi-additive technology comprises a group of metal deposition processes for which an adhesion and seed layer are deposited followed by a lithography step for the pattern definition, followed by an electro-plating step into the resist openings. Finally, the resist is stripped and the seed and adhesion layer are removed by wet or dry etching. In step 5 the silicon recess with a nominal depth of 350 μm is created by dry etching using a thick photo resist as masking layer. In the next step 6 getter (indicated with pink color) is deposited inside the cavity next to the later optical path. As indicated also in step 6, it would be possible to deposit also ARC at the bottom of the etched recess using dedicated masking techniques to protect the surface areas, but this option was not considered here.

In the final step 7, mechanical dicing is performed to pre-separate the cap structures from surrounding regions. The dicing is only done through the silicon and only slightly into the carrier to keep the wafer robust for the following wafer bonding step. The regions around the caps correspond to the areas on the device wafer were no cap structures are required. Those regions have the sputtered metal layer on the glass carrier wafer under the bond interface, which will later block the laser and prevent their detach from the carrier wafer. Based on that, only the cap structures can be released from the carrier wafers, whereas all other structures remain on them. The condition in step 7 shows a so-called “cap donor wafer” with prepared cap structures, which is ready for wafer bonding with the corresponding device wafer and subsequent detach of the cap structures by laser assisted de-bonding. Real images of such a cap donor wafer with monolithic caps are shown in Figure 3.
B. Fabrication of Hybrid Silicon Caps

The preparation of hybrid cap structures is outlined here as option for the maximization of volume to be encapsulated. Core of the concept is to create the caps from two parts, which constitute of a silicon frame and a flat lid. The fabrication flows for both components are shown schematically in Figure 4 with the flow “A” indicating the process for the frame and flow “B” indicating the lid process. The silicon frame is fabricated from a standard 725 μm thick silicon wafer enabling a maximized cavity height of the final caps. In a first step, the frame wafer receives Au rings on its front side using a semi-additive process. After this, the side with the Au rings is bonded with temporary adhesive to a glass carrier wafer. Now, the wafer back side is polished, a thin silicon oxide deposited and a second semi-additive process is done to deposit Au rings also on the back side of the wafer. The proper location of the rings in relation the structures on the front side is ensured by front to back side alignment of the resist lithography step. As a final step of the frame preparation sequence, a further lithography step with thick photo resist is done followed by rapid silicon dry etching, which etches completely through the thick wafer and removes all silicon except the frame features.

The preparation of the silicon lid works similar, as the preparation of the monolithic cap in the previous chapter. Only difference is, that formation of a recess was not done here. However, this would be possible and is an additional option to further increase the final encapsulation volume of the hybrid caps, if required. As seen in flow “B” of Figure 4, also here the silicon wafer is prepared with anti-reflective coating and bonded temporary to a glass carrier wafer with prepared structured metal layer for later blocking of the laser radiation. After temporary wafer bonding, the silicon wafer is thinned to 300 μm, polished and anti-reflective coating is deposited. Following, semi-additive deposition of Au+Sn is done to create the bond rings and getter is deposited. In the final preparation step, mechanical dicing is performed to separate the lids from surrounding regions. Also here, dicing is done through the silicon and only slightly into the carrier wafer. In the next step the hybrid caps are formed by bonding the silicon frame to the silicon lids. This is done by using face to face wafer alignment followed by an AuSn wafer bonding sequence. The wafer bond process enables melting of the AuSn bond rings, by forming an eutectic phase reacting and joining with the Au rings on the other side leading to the conversion into a joint ring composed of an AuSn core surrounded by remaining Au sockets. This allows the establishment of robust and air tight metal sealings with increased re-melting temperature. Finally, only the carrier from the silicon frame wafer has to be removed as shown in step 7. This is done by laser assisted de-bonding followed by solvent and plasma cleaning of the remaining adhesive. Figure 5 shows images of a fully prepared donor wafer with hybrid caps. The silicon frames with their large height can be well recognized in the right image.
C. Fabrication of Hybrid Caps with Germanium Lids by Reconfiguration Method

As germanium has much better IR transmission capability as silicon for LWIR range, this option for the creation of cap structures with germanium lids is presented here. The related process flow is shown in Figure 6. The flow A is identical to the previous chapter and describes the fabrication of silicon frames from silicon wafers with 725 μm thickness. The flow “C” on the right side shows the preparation of carrier wafers with germanium lids, which can be bonded then to the silicon frames.

Figure 6: schematic fabrication flow for donor wafers with hybrid germanium caps

Starting condition in step 1C are 150 mm germanium wafers with thickness of 225 μm and 200 mm glass carrier wafers. First, thick metal rings of Au+Sn are deposited on the germanium wafers by a semi-additive process followed by deposition of getter. (step 2C) On the carrier wafer, a thin metal layer is deposited by sputtering and structured by wet etching to create local and global alignment marks. The carrier wafer is then prepared with the temporary adhesive layer. After singulation of the germanium wafer (step 3C), the germanium lids are die bonded with their back side to the carrier wafers. (step 4C) The die bonding is done with reference to the local alignment marks, which indicate the required placement positions to match their locations and step & repeat pattern with those on the frame wafer. For precise placing, a local recognition can be optionally performed by each bond position, permitting basically local fine adjustment. After removal of the temporary adhesive next to the germanium lids (step 5C), the silicon frames are aligned and bonded to the germanium lids. (step 6) The left image in Figure 7 shows a carrier wafer with die bonded germanium lids according to condition 5C in Figure 6. The global alignment marks on the carrier wafer of the lids are used to position frame and lid wafer. The used AuSn wafer bonding process is the same as used for the bonding of the hybrid silicon caps in the chapter before. As remaining step, also here the carrier wafer has to be removed from the frame side followed by adhesive cleaning to get the wafer ready for later bonding to the device wafer.

Due to the CTE mismatch between germanium and silicon as well as the B33 glass carrier wafers special attention has to be drawn to stress conditions created during and after cooling steps of the AuSn bonding process. The thermo-mechanical stress can exceed easily fracture strength of the involved materials especially, if such laterally large cap structures are joined as in this example. The right image in Figure 7 shows a germanium lid after the wafer bonding sequence and carrier removal step were performed. It can be recognized easily, that cracks are present in the lid, which result from high thermo-mechanical stress. Based on this, it was concluded, that the hybrid germanium cap formation is not applicable for the large lateral dimensions of the here required cap structures. But it is most probably a very promising approach for the fabrication of cap structures with smaller dimensions.

Figure 7: left: carrier wafer with reconfigured germanium lids according to Figure 6 / picture 5C; right: germanium lids after bonding to frame wafer / cracks visible due to large dimensions and mismatch in coefficient of thermal expansion (CTE)

IV. VACUUM TIGHT TRANSFER BONDING OF CAP STRUCTURES FROM DONOR WAFERS TO DEVICE WAFERS

In order to enable a bonding of the cap structures from the prepared donor wafers to the device wafers, those have to be prepared with suitably bond ring structures first. In the described capping technology all cap structures have Au rings as bond interface, which require rings of Au+Sn on the counterpart / receiver side to enable the later soldering process of the caps. Based on this, all device wafers have to undergo a related electro-deposition process to form the Au+Sn rings, which was done by semi-additive technology in these experiments. Semi-additive processing involves sputtering of a seed layer,
lithography, electro-plating, resist removal and seed layer etching. All these processes interact with the wafer surface and are not allowed to be applied on wafers with released/freestanding bolometers, which are tiny fragile thin MEMS structures as soon as the sacrificial layer supporting them is removed from the wafer. However, it was possible to shift this bolometer release to the very end of the process chain. Thus, the semi-additive process could be done before the removal of the sacrificial layer and before the microbolometers became freestanding and fragile. Figure 8 shows images of a bolometer wafer after formation of the Au+Sn bond ring structures.

The schematic process flow in Figure 9 shows the final transfer bonding of monolithic and hybrid silicon caps from the donor wafer to the device wafer, leading to the sealing of the MEMS. The counting of the steps starting from 8 continues the counting of the steps in Figure 2 and Figure 4. In step 8, both wafers are aligned using marks, which were created with the deposition of the Au and Au+Sn on the wafers.

In step 9, the AuSn wafer bonding sequence is executed. In that step the AuSn on the device side is melting and wets the Au on the cap side. An eutectic liquid phase is formed homogeneously over the extension of the frames, reacts with the Au counterpart and solidifies, at latest by cooling. In case of the hybrid cap the already existing soldered AuSn frame won't remelt due to the higher melting temperature of the already fully transformed solder into the Au rich phase Au5Sn.

In step 10, the carrier release process is performed, selectively liberating the caps. To enable this, laser exposure is done on the entire wafer from the glass carrier side. Due to the presence of the light blocking metal layer at the bond interface in the areas next to the caps, the adhesive cannot be exposed here. But in all areas were caps are present, the light blocking layer is missing so that the adhesive can be exposed at those positions. Based on that, the caps can be selectively de-bonded from the carrier wafer to remain on the device wafer and all other regions are taken away with the carrier wafer.

In the final step 11, the remaining adhesive is removed by wet cleaning using solvent or dry-cleaning using plasma. Figure 10 shows and example of a bolometer wafer with bonded monolithic caps, which was produced using the discussed process sequence. The Figure 11 shows exemplary a cross section of a microbolometer device, which was sealed with a monolithic cap.
After sealing, the device wafer was finally diced in single chips. The yield of sealing after full processing was at that point evaluated on the basis of the visible cap deflection of the silicon roof, leading to a process yield estimated by around 97%. A real image of cap deflections as well as optical deflection measurement result and yield map are shown in Figure 12.

The sensors corresponding to this design show good sensitivity of pressure below 1000 Pa. Due to the current limit of the available vacuum pump, we could only characterize the sensor response at pressures down to ~10 Pa (0.1 mbar). For measured electrical resistances beyond the range of 99–165 kΩ (see Figure 13), we can only indicate whether an encapsulated chip has a pressure beyond the pressure range of 10-1000 Pa. Further work is ongoing to characterize the micro-Pirani sensors at lower pressure, targeting a complete master curve for the further low-pressure domain.

The vacuum sealed MBA-on-ROIC samples using the monolithic caps, with and without getter material, were characterized with regards to the vacuum level inside the packages. The resistances of the micro-Pirani sensors corresponding to the design presented in Figure 13 were measured for a sample set with different cavity sizes and getter surface. Those measurements are summarized and shown in Figure 14.

The results show average electrical resistances as low as 100 kΩ and 140 kΩ for samples with and without getter, respectively. These correspond to vacuum levels as low as 10 Pa (0.1 mbar) for samples without getter material, it means at the minimum limit of the reference curve, and 220 Pa (2.2 mbar) for samples without getter materials. The results demonstrated the impact of getter material in reducing the pressure level in the packages.

Each sealed sample includes two micro-Pirani test structures (placed on top and bottom part of each microbolometer array), showing variation/deviation up to 10 kΩ between both (similar deviation to Figure 13) for a same sample, probably resulting from MEMS fabrication tolerance. These double DUT per sample permit to identify a visible trend between samples from wafer center and wafer edge, last presenting higher pressure levels, probably caused by radial outgassing from wafer surfaces, with cumulation of outgas flow towards wafer edge during the wafer bond process. The cavity designs seem less

V. CHARACTERIZATION RESULTS OF BONDED SAMPLES

The operation principle of micro-Pirani devices allows the electrical resistance across the sensors to vary according to a certain pressure level. Micro-Pirani sensors integrated within the microbolometer structures have been characterized inside a vacuum chamber. The objective was to obtain a master/reference curve for the micro-Pirani sensors, showing electrical resistance of the sensors corresponding to certain pressure levels. The master curve (i.e. reference curve or sensitivity curve) of one promising sensor design is shown in Figure 13.

![Device wafer with deflected caps after singulation](left) and hermeticity yield evaluation of 97% (right) on the basis of visible deflection of 300 μm thick silicon cap roof (center)

![Behavior of micro-Pirani sensors corresponding to a promising design under various pressure levels between 10 and 1000 Pa](left) / pressures are shown in logarithmic scale
sensitive/prompt to the sealed vacuum level, however a maximized inner volume being apparently more advantageous for lower inner pressure. Since the different sizes of getter surface do not reflect in perceptible differences, the possible outgassing can be supposed rather of inorganic nature. At the submission deadline of this manuscript the evaluation of the hybrid cap structures and related sealing results was still under investigation. However, a similar performance compared to the monolithic caps is expected.

VI. CONCLUSION

Wafer level capping was adapted for vacuum sealing of ICs with microbolometer arrays having large lateral dimensions of 13.6 x 13.1 mm². The required cap structures with lateral dimensions of 12.3 x 11.2 mm² were created in different ways using a monolithic and a hybrid approach. The vacuum sealing was enabled by wafer bonding using AuSn soldering of the caps utilizing frame structures of Au and Au+Sn, which were deposited by electro-plating on cap and device side respectively.

In case of the monolithic cap fabrication process, standard silicon wafers were used to create caps structures with seal rings and cavity. To enable a selective device capping, the silicon wafer was temporary bonded to a carrier wafer and the caps were pre-singulated on it. After wafer bonding of the caps to the device wafer, the temporary adhesive bond was released at the back side of the caps by laser assisted de-bonding. As a result, the caps remain on the device side, whereas all other structures remain on the carrier wafer. The so-called “selective capping” enables to cover only a portion of the device so that peripheral zones e.g. with IO pads are still accessible.

The case of the hybrid cap fabrication process, the cap structure was created by soldering a silicon frame to a silicon or germanium lid first. The hybrid caps can then be bonded to the device wafer and released from the temporary carrier wafer in a similar way as the monolithic caps. It was shown, that the fabrication of hybrid caps with germanium lids produced cracks in those. Reason for that was the CTE mismatch between silicon and germanium and the created thermo mechanical stress at the given large lateral dimensions. However, the approach is promising in cases, if smaller cap structures are required for a similar application.

After the final capping process, especially the monolithic caps were characterized regarding their hermetic sealing capability. For that, Pirani test structures, which were also located on the microbolometer devices, were utilized. Related test structured were measured first in non-capped state in a test environment under defined vacuum conditions. The resulting resistance vs. pressure behavior was later compared with measurements of identical Pirani structures on capped devices. Based on this approach, final vacuum levels of 10 Pa (0.1 mbar) and 220 Pa (2.2 mbar) could be determined for devices with and without getter respectively.

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