Demonstration of Eight Metal Layer Redistribution on Glass Substrate with Fine Features and Microvia

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Abstract— **With increasing need for computing power, there is a demand for higher performance packaging that can enable faster communications. A promising candidate for many high-performance packaging applications is glass substrates with fine-feature (≤2 µm lines and spaces) redistribution layers. Georgia Tech's Packaging Research Center has done extensive work on glass substrate packaging, and in this paper, we have developed a baseline process with optimized processing conditions to increase the number of metal layers fabricated on glass cores (substrates), and in this way increase the I/O density and performance.**

Double-side processing means performing processing steps on both sides of the substrate at once, rather than completing one full layer on top and then starting the bottom layer. This way of processing can eliminate the need for a carrier wafer and hence reduces the number of steps as well as complexity of processing. Fabricating high-density wiring on both sides of the substrate is beneficial in that it can reduce total layer count and create a more symmetric package which will reduce substrate warpage, and when combined with through glass via (TGV) substrates can significantly reduce the interconnection length. Furthermore, by balancing the amount of metal and polymer on either side of the substrate, total stress can be minimized. Glass is chosen as a substrate for the work presented in this paper owing to its compatibility with double-side processing and its availability at various panel sizes with and without TGVs. The dimensional stability, high planarity, and relatively low cost of glass makes it an attractive material for this application.

In this paper, fabrication of an eight metal layers (8MLs) test vehicle on glass core is demonstrated by performing a thorough optimization of processing steps described in the process flow. Fabrication is performed on 300 µm thick 6" x 6" glass panels with < 20 µm diameter microvias, 15 µm line (L) and 15 µm space (S) features on the inner metal layers, and 2 µm L/S on the outer-most metal layers on the top and bottom. The optimized fabrication method involves a standard semi-additive process (SAP) for the inner metal layers, and an advanced semi-additive process (aSAP) using sputtered seed layer for the outer metal layers. Femtosecond laser based microvia fabrication will be presented where the fabricated via diameters are limited only by the laser spot size, and the heat affected zone (HAZ) will be minimized. Optical images measured using a 3D step profiler of samples at multiple stages of fabrication will be presented, along with the SEM images of the completed fine features on the outer-most layers.

Keywords—redistribution layers, microvias, multi-layer structures

I. INTRODUCTION

With constantly increasing need for high performance computing, there is a need for faster chip-to-chip communications. As Moore's Law slows down while demand for high-performance and low cost continue to grow, there is a growing need to enable heterogeneous integration at the package level [1]. A promising candidate for increasing chip-to-chip communication speed is glass based interposers with fine features and microvias having critical dimensions similar to that of the L/S to enable high data transfer rate between multiple dies mounted on the same package. Glass based packaging is cheaper than silicon, because glass has tailorable CTE, and better electrical properties [2]. Having a tunable CTE is attractive because it can be tailored to a value that can minimize thermal stress build-up of the package. Mukhopadhyay et al. have demonstrated through simulations that glass interposers will have higher data rate and lower energy per bit than silicon interposers with the same feature size [3]. However, manufacturing/processing for glass substrates is not as mature as that for silicon substrates, and so glass substrate packaging cannot fulfill its potential due to process challenges. One of the biggest limitations so far is the layer count on glass substrates. The aim of this work is to demonstrate a baseline process for eight metal layers on glass substrates to identify and overcome challenges related to increasing the layer count on glass substrates.

Fabricating circuitry on substrates necessarily adds stress to the substrate by adding material. To minimize warpage of the substrate, the substrate may be bonded to a carrier wafer, or equivalent amounts of material may be added to both faces of the substrate at the same time. Double-side processing means completing each process step on both the top and bottom of the substrate before moving on with the next step. Fabricating high-density wiring on both faces of the substrate is beneficial in that it can reduce total process steps for a given layer counts and create a more symmetric package which will reduce substrate warpage. Also, eliminating the need for a carrier wafer will reduce the complexity of processing which requires additional steps. Another reason why glass is attractive as a substrate is due to its compatibility with double-side processing. The dimensional stability and high planarity of glass, as well as the relative ease of fabricating through-substrate vias make glass highly compatible with double-side processing.

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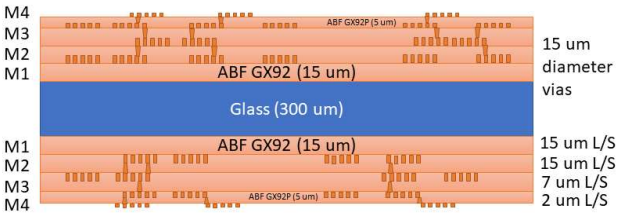

Fig. 1. Model cross-section showing 8ML specifications.

A model cross-section of the fabricated samples is shown in Figure 1. The substrate used was 300 µm thick, 6"x6" glass panel with CTE of 7.8 ppm from Corning (Corning, NY). The outer-most metal layer (M4), has the finest features to enable fast horizontal communications for chip-to-chip data transfer. Finer features enable faster communication because smaller wires increas interconnect density, which increases data transfer rate. For ease of processing and to promote higher yield, the other metal layers (M1-M3) had larger features and used a different photoresist than M4, as feature size was not as crucial. As the design used was symmetrical, naming convention will be used where M1 is the 1st metal layer fabricated (the innermost layer), on both the top and bottom of the substrate.

II. Process

A flow-chart of the SAP process is shown in Figure 2. RDL wiring for the inner six metal layers (M1to M3 at both top and bottom side of the glass substrate) for this demonstration is done with semi-additive processing (SAP). The first step is a surface treatment to promote adhesion of the dielectric to the substrate. Then, a vacuum laminator (Meiki, Japan) is used to laminate the build-up dielectric onto the glass panels. The build-up dielectric for M1-M3 is chosen to be ABF GX92 from Ajinimoto, Japan. Due to poor adhesion of copper to glass, dielectric is added even for the first metal layer. In layer M2-M4, microvias are drilled with a femtosecond laser micromachining system from OPTEC, Belgium. The spot size of the laser on the femtosecond drilling tool is 20 microns, which limits the achievable via size to around 15 microns. The seed layer was chosen to be solution-deposited electroless copper with chemistry provided by Atotech, UK. A negative tone dry film photoresist (DFR) with 15 µm thickness from Hitachi Chemical (now Showa Denko) Corp is used for M1 and M2. M3 uses the same resist with similar conditions but at a 7 µm thickness. The negative tone DFR from Hitachi Chemical did not require a pre-exposure bake or a post-exposure bake, which made double-side processing simple. Exposure of the 15 µm DFR was performed on a Tamarack mask aligner, while exposure of the 7 µm DFR was done on a maskless aligner from Heidelberg Instruments, Germany. Development of exposed negative-tone Hitachi resist was done in a spray conveyor system at 30 ºC for a time of 25 s for the 7 µm resist, and a time of 42 seconds for the 15 µm resist. Electroplating was performed in a sacrificial anode tank with chemistry provided by Atotech, UK. Beaker-scale stripping was performed under the following conditions: 5 minutes at 40 ºC in a bath of EKC-162 from EKC. Seed layer etching was performed in a spray conveyor system at 30 ºC for a time of 25 s.

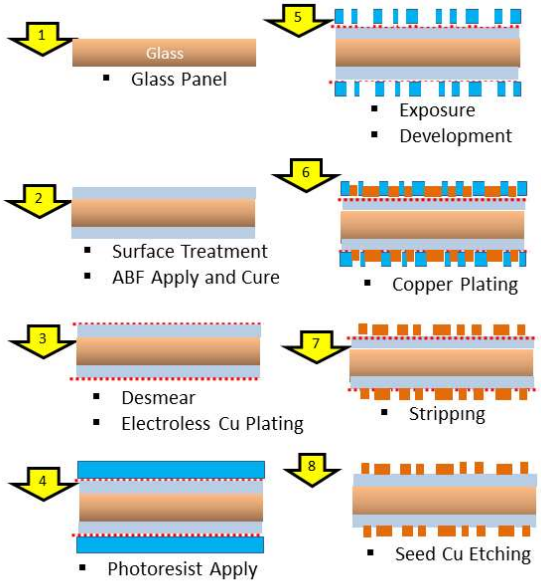

Fig. 2. Process flow for semi-additive process.

For M4, to enable finer features, some process and material changes were necessary. Sputtered seed layer was chosen instead of electroless seed layer to help reduce the surface roughness and improve the adhesion of very fine features. Sputtering was done in a DC sputter chamber with multiple sources so the Ti and Cu could be deposited without breaking vacuum. 0.2 A of current were used in the sputter chamber from Denton Vacuum, USA. A different dielectric was also chosen to improve fine features. ABF GX92P is thinner and has smaller fillers than ABF GX92. These smaller fillers decrease surface roughness which leads to an improvement in resolution during lithography. There should also be a corresponding decrease in microvia size due to smaller fillers and less thickness, however this was not realized due to the spot size of the laser. A new photoresist was also necessary to achieve higher resolution. For M4, a 5 µm positive tone DFR from TOK (PC-0471W-F5) was used (Tokyo Ohka Kogyo Co., Japan). The positive-tone resist required both pre- and post-exposure bake, which made processing challenging. Due to concerns with placing PR directly onto the surface of a hot plate, both bakes were done in a convection oven. The temperature and time for both bakes were increased slightly for this work due to reduced heat transfer in oven as compared to hot plate. It is important to note that the optimal bake conditions for each oven and are different. An attempt to change ovens while maintaining temperature and time constant resulted in drastically reduced quality of lithography. Exposure for the 5 µm DFR was performed on a MLA 150 maskless lithography system from Heidelberg Instruments, Germany. Developing was done beaker-scale in 2.38 % TMAH (tetramethylammonium hydroxide) at 30 ºC for 90 seconds. Stripping was done beaker scale in the same EKC photoresist stripper for 4 minutes at 40 ºC.

III. Results

The minimum feature size that could be achieved with the Tamarack mask aligner, due to the tool's incompatibility with glass masks, was 15 µm line and 15 µm space (15 µm L/S). The design for M1 had landing pads for microvias, and some blocks of 15 µm L/S to show the resolution. Pictures of the 15 µm L/S from the completed M1 is shown in Figure 2. During the processing, pictures were taken using a Keyence VX3600 laser confocal scanning microscope (Keyence, USA).

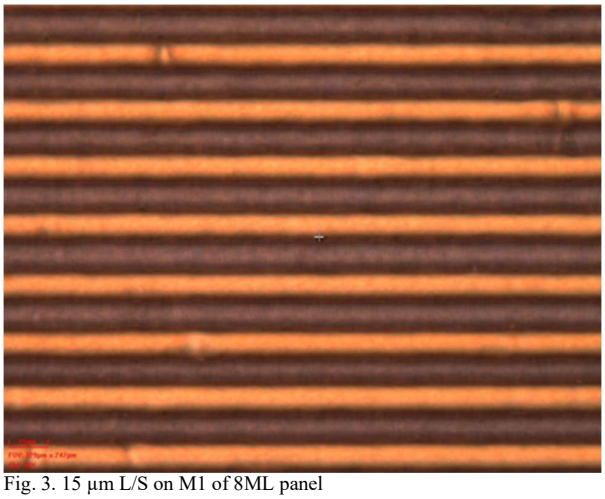

Fig. 3. 15 µm L/S on M1 of 8ML panel

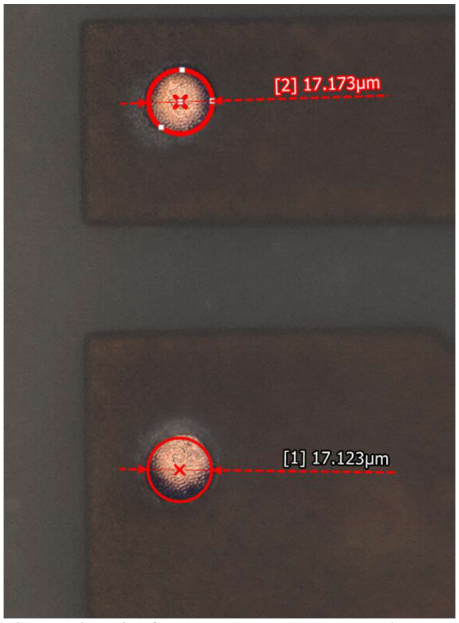

Fig. 4. Microvias from M2 to M1 on 8ML panel

M2 was fabricated with the same conditions as M1, with the addition of microvias. Examples of the microvias from M2 to M1 are shown in Figure 4. The minimum resolution of the microvia diameter achieved was 17 µm. For M3, using the 7 µm thick DFR, the minimum feature size resolution achieved was 5 µm L/S, which is shown in Figure 5. The target L/S was 5/5 and the achieved L/S was 4/6 microns due to minor process variations. Other than this change in resolution from M1 and M2, with a corresponding change in plated copper thickness, the results for M3 were the same as the results for M2 and M1.

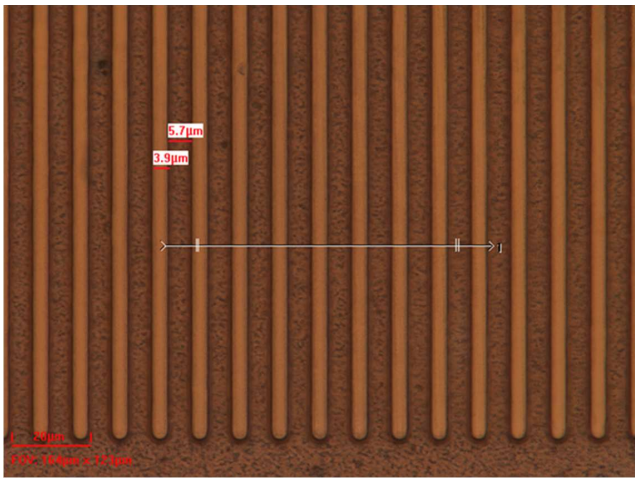

Fig. 5. 5 µm half-pitch wiring from M3

M4 fabrication proceeded, using maskless lithography and the TOK positive-tone DFR. Even though the dielectric thickness was reduced from M1-M3, the via size was still limited to ~15 microns due to the spot size of the laser. The well resolved 2 µm features after seed layer etching are shown in Figure 6. In the optical image, the line width is measured to be 1.8 µm, with a target value of 2 µm.

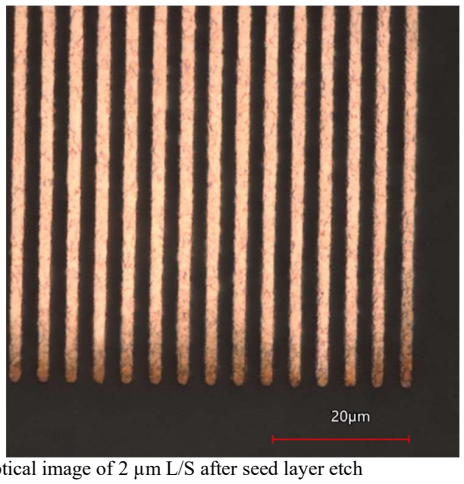

Fig. 6. Optical image of 2 µm L/S after seed layer etch

An SEM micrograph of 2 µm features on M4 is shown in Figure 7. This image was taken after seed layer etching. The width of the copper traces in the SEM micrograph is measured to be 1.98 µm, with a target value of 2 µm width. The SEM and optical images were taken at different locations on the panel, so the discrepancy in line width is likely due to differences in local exposure and seed layer etch conditions.

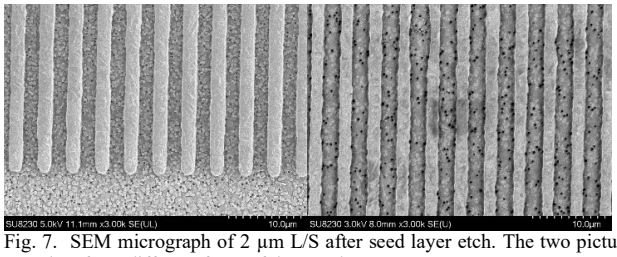

Fig. 7. SEM micrograph of 2 µm L/S after seed layer etch. The two pictures are taken from different faces of the panel.

Cross-section images will now be presented from different locations on the panel. Figure 8 shows cross-section images from two different locations on the panel, one from a via structure, and the other showing fine line features on different metal layers. The left side of Figure 8, taken at 150×, shows a microvia from M3 to M2. The right side of Figure 8, taken at 50× shows 15 µm L/S on M1 and M2, as well as 3 µm L/S on M4.

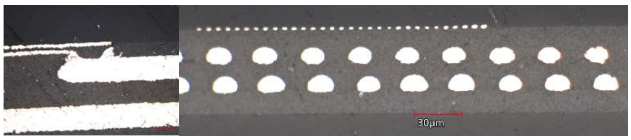

Fig. 8. Cross-section images showing multilayer structures on one face of the panel. Left) M1-M4 from one side of panel. Microvia is from M3 to M2. Right) M1, M2, and M4 showing 3 µm L/S on M4 and 15 µm L/S on M1-M2.

Via chain structures with 50 microvias were measured to have a resistance of 1-2 Ω. Literature reports similar structures with 400 microvias of 5 µm diameter were measured to have a resistance of 12.5 Ω [4]. Assuming resistance from pads and traces is negligible, the 15 µm vias in this work are approximately as resistive as the 5 µm vias, probably because the cross-section of the 15 µm vias are not fully filled with copper, as seen in Figure 8.

IV. Discussion

Some of the challenges during fabrication included alignment, adhesion issues due to the multi-layer stress, and warpage of the substrate due to multi-layer stress. The alignment issues were mostly due to the specific tools being used, as the femtosecond laser drilling tool had some issued with calibration of the stage, and the mask aligner used on M1 and M2 had some problems with the vacuum holding the mask steady.

There were some serious issues with adhesion of some regions of seed layer, as shown in Figure 9. 5% of the ground plane structures on M1 delaminated from the dielectric layer beneath during fabrication of M4. There did not appear to be any pattern to which coupons had these delamination issues, so it is most likely due to local irregularities in the electroless seed layer deposition. These irregularities could be caused due to surface defects or contamination in the dielectric. However, it seems as though the multi-layer stress of these 8ML panels is starting to exceed the adhesive strength of the seed layer. Applications requiring four metal layers on one side (or more) should use sputtered Ti/Cu seed layer rather than electroless seed layer, as this will increase the adhesive strength [5]. Although the majority of the coupons using the electroless seed layer survived to finish M4 fabrication, reliability will be much improved by increasing adhesion strength of the seed layer to the dielectric. Adhesion of the 2 µm features on M4 was also a concern, as some of them peeled off with the dicing tape during singulation. This issue was fixed by applying photoresist before dicing to prevent the lines from contacting the tape, but poor adhesion of fine feature RDL remains a concern.

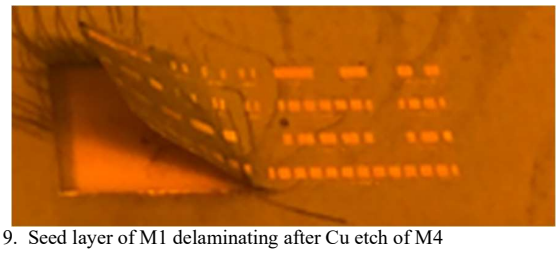

Fig. 9. Seed layer of M1 delaminating after Cu etch of M4

In general, warpage was relatively minimal, because the material added to each face of the panel was equal. There was no warpage visible to the naked eye, although there was some warpage that could be detected by the maskless lithography tool when exposing M4. This warpage had some effect on the resolution at different spots on the panel, as shown in Figure 8.

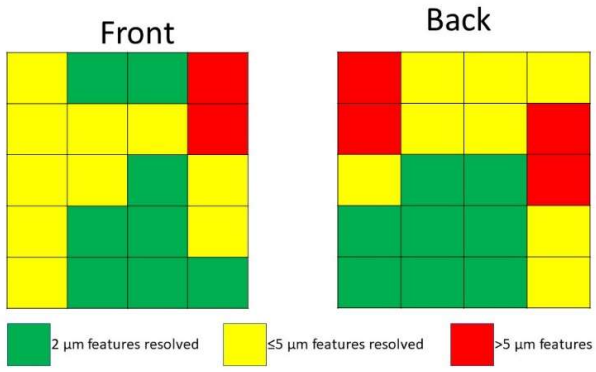

Fig. 10. Resolution by coupon for M4 of one completed panel

Figure 10 shows that the areas with 2 micron resolution were concentrated in the same areas on both faces of the panel, indicating that this region is relatively flat, while the other regions have warped out of focus of the maskless aligner. The bottom right coupons of the front and the bottom right coupons of the back are in the same region of the panel, as the pattern is mirrored across the y-axis when exposing the back vs the front. The depth of focus of the maskless aligner is only 25 microns, which seems to restrict the successful resolution of 2 micron features to areas of the panel that are relatively flat. The vacuum on the stage of the maskless aligner was unable to overcome the warpage because the panels were very stiff with eight layers of dieletric applied to them. We believe with the introduction of real-time auto focus options to the Heidelberg MLA 150 tool, the yield could be enhanced by minimizing the effect of warpage.

V. Conclusion

Overall, a process was developed to address some of the challenges facing the implementation of glass core interposers with high density interconnects for high performance computing applications. A process for double-side maskless

lithography to achieve ≤ 2 μm features is demonstrated on glass for the first time. This work has demonstrated a baseline process for fabricating multi-layer structures with fine features and microvias and may be easily extended to more than eight layers if desired. The only concern with going above eight layers is the adhesion of the seed layer to the dielectric. This work represents another step towards glass becoming competitive in HPC and heterogeneous integration applications, having both fine features and many layers. Further work will be to integrate through-glass vias and evaluate reliability using tests such as HAST.

VI. Acknowledgements

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VII. References

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