

Reliability in Selective Thinning Technology of Solder Resist for New IC Substrate Architecture

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Abstract— This paper presents a reliability aspect of the solder resist (SR) thinning technology. The resist thinning (RT) process was developed for thinning down SR layer highly uniformly at a large panel scale. By combined with photolithography process, the RT process can thin down SR materials selectively and can form multi-step structures. This paper first describes what the RT process is and what kind of benefit can be brought by applying the process. Then comparative studies in the impact of the RT process on SR material performances, such as surface morphology and material reliability, are reported. From the reliability study, it was revealed that the insulation reliability of SR materials was not impacted by applying the RT process. This research indicates that RT process is a beneficial tool for new SR structuring, without compromising materials performances.

Keywords—Solder resist, thinning, Wet etching, Multi-stepped structure, material reliability

I. INTRODUCTION

Higher functionality and smaller size are the keys in evolution of electronic devices. To meet the growing demand, IC packaging needs to possess integrated functionality in a small form factor and high reliability. The requirement of packaging integration drives the development and the implementation of advanced packaging technologies, such as package-on-package (PoP) [1-3], multi-chip modules [4-6], and system-in-package [7-9]. These technologies apply multi-layered packaging substrates with quite high-density Cu traces, build-up dielectrics, and SR layers with fine pitch assembly pads, to achieve high in and out (I/O) signal density. State-of-the-art SR materials with remarkably high resolution can form fine-pitch solder resist opening structures [10,11], however, current patterning process with standard photo-lithography only can define one or zero: SR open or non-open features in the SR layers.

To overcome this limitation, a new resist thinning (RT) process technology was developed and introduced for selectively thinning down SR layer uniformly. The RT process enables formation of half-etched SR structure at a large scale. By applying the technology, variety of new 3D structures of SR materials can be formed, such as partial Cu pad exposure, SR dam structure, and multi-step SR structures. These new SR structures are highly beneficial to resolve several technical

challenges such as pad lifting, shorting by surface finish, solder bridging, void formation during underfilling, underfill overflow, and SR undercutting. In the previous paper [12], detail mechanism of the RT process was reported and the fundamental schematics that enables uniform SR etching was discussed. Also, a comparative studies between the RT process and standard development process were conducted to reveal how accurately the RT process can thin down the SR materials, which is vital for half-etched SR structure formation.

While the half-etched SR structures formed with the RT process are attractive for many applications, there was no research on the material performance of the “half-etched” SR materials. Therefore, this paper studies the impact of the RT process on SR surface topology, as well as their reliability. After briefly reviewing the RT process schematics and the capability of the process, this paper discusses the impact of the RT process on the SR materials performance. First, comparative analysis of SR material surface was conducted. Surface roughness and wettability of the SR material were compared between non-etched surface process with a standard development, and half-etched surface processed with the RT technology. After the first study, reliability test was performed to visualize the impact of the half-etching process. Biased-highly accelerated stress test (BHAST) reliability was conducted to see if there would be any change in insulation reliability of SR materials.

II. FUNDAMENTALS IN RESIST THINNING (RT) PROCESS

Basic process flow of the RT process, including three steps, is illustrated in Fig. 1.:

1. 1st tank: dipping into Chemical A to swell SR materials from the top surface
2. 2nd tank: spraying Chemical B to remove the swollen part of SR
3. Rinse tank: spraying water rinse to clean the remaining SR surface

Dipping process in the first step is the key to achieve highly uniform SR swelling from the top surface, based on the chemical diffusion in the SR. In the 2nd tank, swollen part of the SR material is etched off. In the final step, water rinsing cleans off very small amount of residues on the half-etched SR. The

substrate shown in Fig. 1 does not have any structures, but RT process works well with substrates that have surface structures such as metal wirings, thin films, and micro-vias.

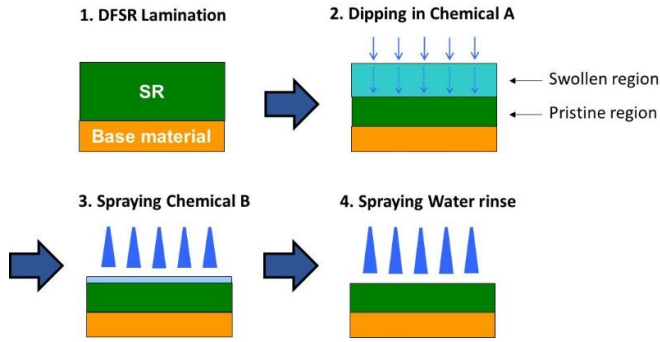


Fig. 1. Fundamental Process flow of RT process

Since SR materials are photo-sensitive/patternable, multi-step patterning of SR materials is enabled by applying multiple time of RT processing with photolithography. Fig. 2 explains the procedure for multi-step patterning. After the DFSR lamination, 1st step is to apply ultra-violet (UV) light exposure for photo reaction, and the RT process is utilized to reduce the thickness of masked area of SR where UV light was not applied. This steps are repeated to thin down the parts of SR layer further until some of the Cu pads are exposed. Then in the final step, the patterned SR layer was fully cured to complete the procedure.

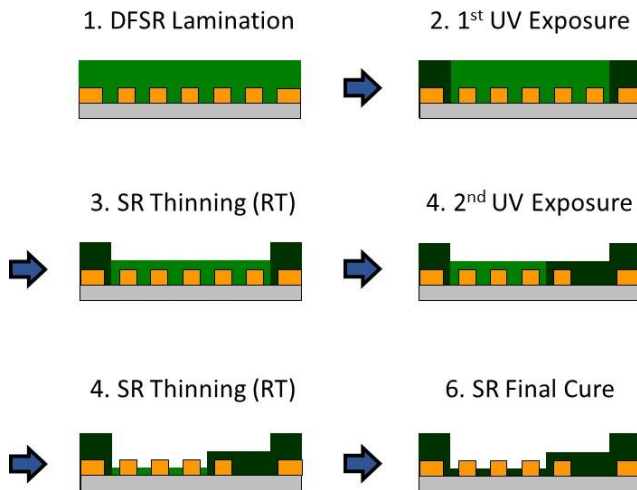


Fig. 2. Multi-step patterning with RT and photolithography processes (light green: unexposed SR, dark green: UV exposed SR)

Demonstrated example of a half-etched SR opening with an exposed Cu pad inside the opening is found in Fig. 3. The Cu pad diameter was 150 μm and the SR opening diameter was 200 μm . Benefit of applying RT process is that keep-out clearance can be minimized, especially when the bump-pitch design rule is very tight.

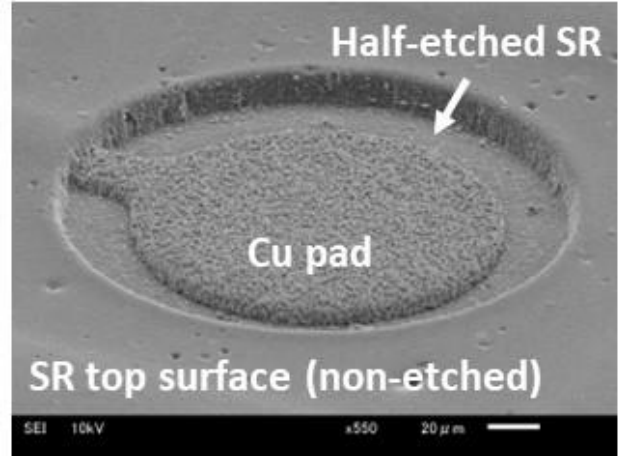


Fig. 3. SR opening with a exposed Cu pad after half etching of SR layer

Fig. 4 shows an example of multi-step structures with partial Cu pad exposure and SR dam structures. Three different height of SR surface can be observed: non-etched surface for SR dam, one-time etched surface for SR plateau, two-times etched surface under exposed Cu pads.

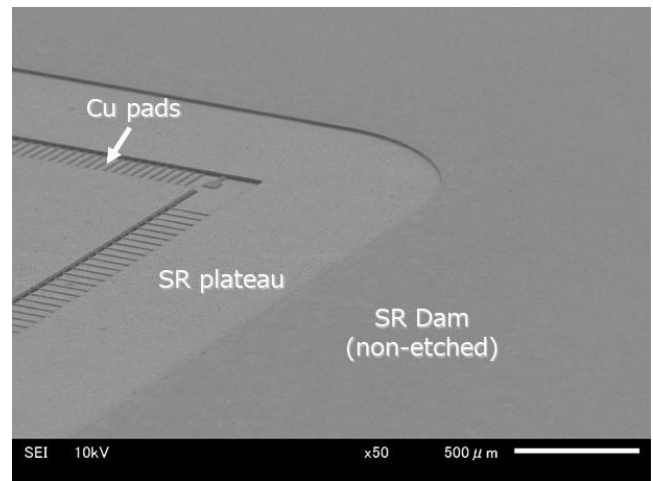


Fig. 4. Multi-step SR structure with partially exposed Cu pads and SR dam

III. SURFACE ANALYSIS WITH RT PROCESS

This section describes the surface analysis of a SR material before and after the RT process. As a SR material for this test, an industry standard dry-film SR material, AUS SR1, was selected. First, SR1 was laminated on FR-4 boards, then the RT process was applied to the SR surface and the SR layer was etched half-way from the panel. After the RT process, UV light was exposed from the top and the panel was introduced to the development process. Finally, the SR layer was fully cured by UV and thermal curing processes. For a reference, an additional board was prepared with the same processes except for the RT process step. After the sample preparation, surface observation and analysis were conducted with the Keyence VK-X100 laser microscope at 2,000X magnification. Fig. 5 shows the surface

appearance of the SR surface with and without the RT process. Bumpy texture is visible on the SR layer with the RT process. In contrast, highly smooth texture of the SR surface is observed on the SR layer without thickness reduction by the RT process.

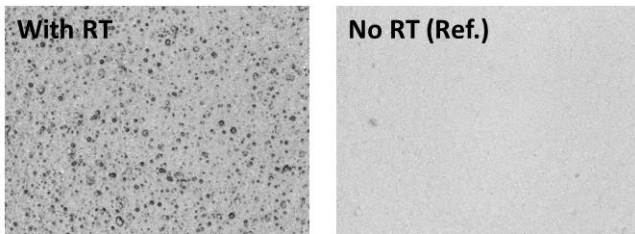


Fig. 5. Surface topology of SR layer with (left) and without (right) the RT process

To see more detail surface texture, scanning electron microscopy (SEM) analysis was conducted from angled view and pictures are seen in Fig. 6. A few micrometer-sized exposed and extruded inorganic filler particles were observed on the SR surface with the RT process. In addition, some porous areas were also observed on the surface where the filler particles had been pulled off during the process. In case of the SR surface without the RT process, much less particles or holes were observed.

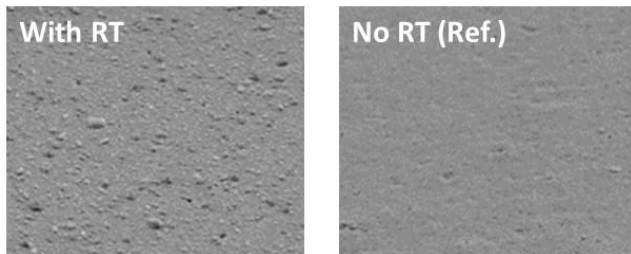


Fig. 6. SEM angled pictures of SR layer with (left) and without (right) the RT process

As speculated from the visual analysis, the SR surface becomes rougher after the RT process. To evaluate the roughness, arithmetical mean height (R_a) values of the boards was calculated from the surface analysis with laser microscopy. R_a is calculated by (1), where l_r is a sampling length, $z(x)$ is a surface profile deviations along the sampling direction [13]:

$$R_a = \frac{1}{l_r} \int_0^{l_r} |z(x)| dx \quad (1)$$

R_a calculation was conducted for three different parts of each board and average value was calculated accordingly. As a result, R_a for the SR surface with the RT process was calculated as 110 nm, and R_a for the one without RT process was 30 nm.

In general use case scenario, plasma process is applied to the substrate boards after the SR curing for surface cleaning. Therefore, impact of the post-plasma process on the surface topology was tested additionally. Ar plasma was applied to the cured SR surfaces by AP-1000 from March plasma systems, Inc. under 200 mTorr of pressure for 60 seconds with various plasma powers at 100 W, 300 W, or 500 W. After the plasma process, surface topology was again observed and R_a values were

calculated in the same way using the laser microscope. The surface pictures with various plasma powers are summarized in Fig. 7. No obvious change in the surface topology was observed after the Ar plasma cleaning processes, regardless of the RT process adoption.

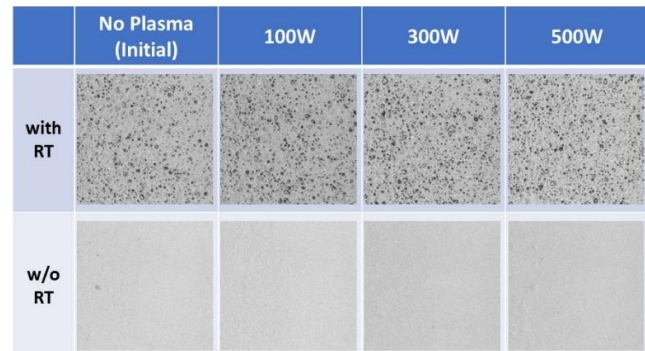


Fig. 7. Surface topology of SR layers after plasma

Fig. 8 shows the roughness factor, R_a of the SR layers with various plasma power conditions. Small fluctuation is seen in the R_a values due to the inherent measurement error in this methodology, but overall trend (dotted lines) indicates that surface roughness of SR layer is highly stable on both with RT or without RT process, regardless of the plasma power.

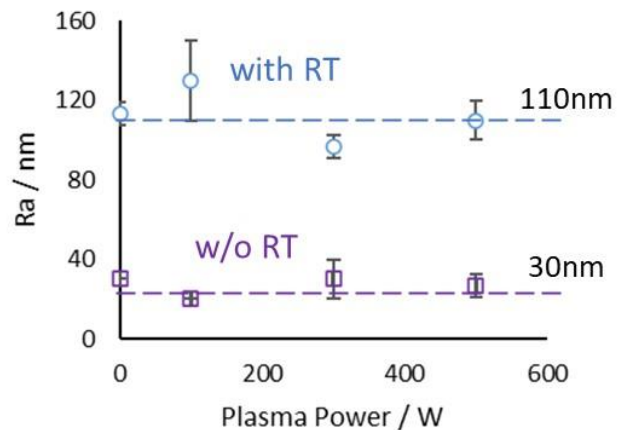


Fig. 8. Surface roughness R_a of SR layers with various plasma conditions for samples with RT process (circle) and without RT process (square)

After the surface analysis, water contact angle measurement was conducted to check the impact of the roughness created by the RT process. Fig. 9 summarizes the contact angle data with various plasma power conditions. Before the plasma treatment, there were about 10 degrees of difference in contact angle between the SR surface with the RT process (~90 degrees) and without the RT process (~80 degrees). The difference became much smaller as stronger power of plasma treatment was applied, and when 500W of plasma treatment was applied, contact angle was the same for both surfaces at 7 degrees. This result indicates that the added surface roughness by RT process enhanced original surface hydrophobicity and led to higher

contact angle, but post-plasma treatment transformed the SR surface into hydrophilic nature and the impact of larger surface by added roughness became negligible.

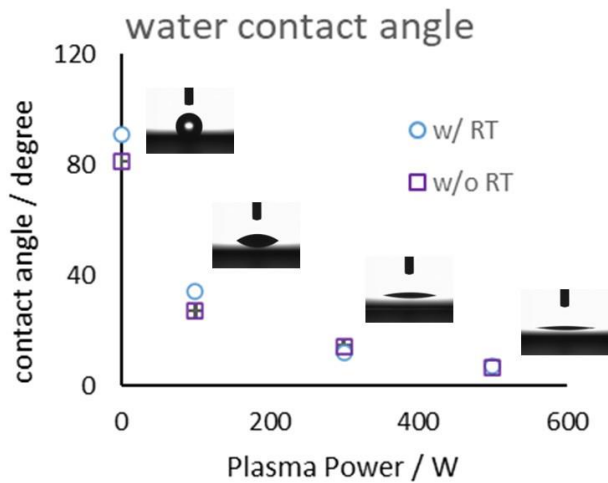


Fig. 9. Water contact angle measurement with various plasma conditions for samples with RT process (circle) and without RT process (square)

IV. RT PROCESS IMPACT ON SR RELIABILITY

This section discusses the study in biased highly accelerated stress test (BHAST) reliability performance of a SR material to evaluate the impact of the RT process on SR material reliability. Sample preparation for this study began with base substrates with $L/S = 12/13 \mu\text{m}$ of Cu comb-like structures, followed by the same SR lamination and patterning processes for each substrate as described in the chapter III. For fair comparison, all the samples were designed to have the same SR thickness at $18 \mu\text{m}$ on Cu structures in the end, whether the RT process was applied or not. To adjust the final SR thickness, SR material with $35 \mu\text{m}$ of in-coming thickness was laminated to the base substrate in the first step, and then thinned down to $18 \mu\text{m}$ thick on Cu by applying the RT process. For the reference sample, $20 \mu\text{m}$ thick SR material was laminated to the base substrate to achieve $18 \mu\text{m}$ thickness on Cu in the end.

Prepared sample substrates were placed in a BHAST chamber, EHS-221MD by Espec Corp. at the temperature of 130°C and relative humidity of 85%. While the substrates were sitting in the BHAST chamber, 5 V of electrical field was applied to the adjacent Cu wirings in the substrates for accelerating Cu migration. Electrical resistance between the Cu wirings were monitored in-situ with AMI-100-S-5 by Espec Corp. to detect when the electrical failure occurs. Failure criteria was defined as $1.0 \times 10^6 \text{ ohm}$ of electrical resistance for the failure detection. 4-5 coupons for each substrate were tested and time to failure was counted accordingly. Fig. 10 shows the Weibull plot of the tested coupons after the failure. As illustrated, trend in life to failure was quite similar for both samples with the RT process and without the RT process. Mean time to failure calculated from the plot was also the same for both samples (375 hours).

This indicates that the BHAST reliability of SR material is not impacted by the application of RT process.

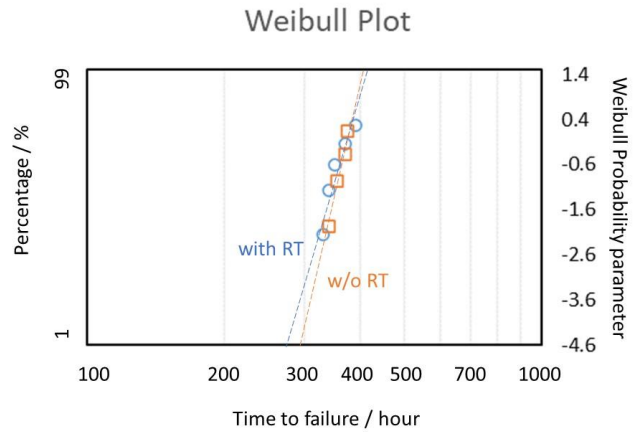


Fig. 10. Weibull plot of time to failure from the BHAST reliability of samples with RT process (circle) and without RT process (square)

Coupons that were electrically failed after 390 hours of BHAST test were further applied to the failure analysis by optical inspection. Fig. 11 summarizes the inspection and Cu cloud formation only at cathode side was observed for both the samples with and without the RT process. Such cloud formation at cathode side is a typical failure mode for BHAST reliability test, based on the reduction of migrated Cu ions whose generation is accelerated at high temperature and moisture conditions. The failure analysis confirms the same failure mode regardless of the RT process applications.

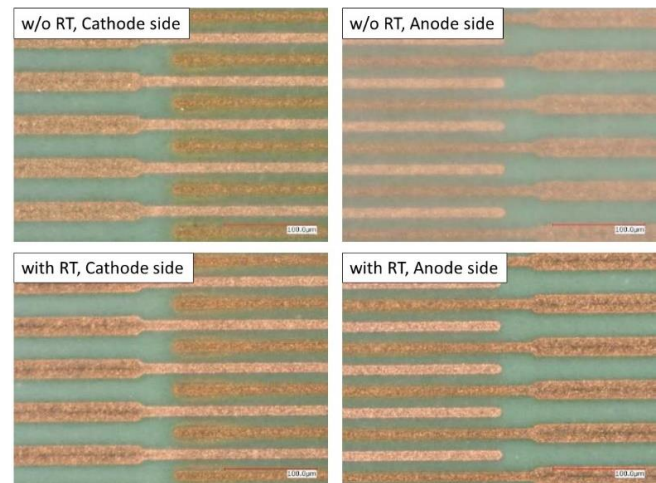


Fig. 11. Failure analysis of the coupons after BHAST reliability test (390h): Cathode (top left) and anode (top right) side of reference sample, and cathode (bottom left) and anode (bottom right) side of sample with RT process

V. CONCLUSION

This paper studied the detail impact of the new SR thinning technology, RT process. Surface analysis showed that the SR surface roughness was increased by applying the thinning process. Higher roughness led to larger water contact angle for RT applied SR surface due to hydrophobic nature of SR material, but post plasma treatment converted the SR surface into highly hydrophilic and the impact of the roughness became negligible after the plasma treatment. Comparable study was conducted to check the impact of the RT process on BHAST reliability performance of a SR material. As a result of the detail analysis, no significant differences in reliability performance nor failure mode were observed between the samples prepared with the RT process or without the process.

In summary, this study revealed that the RT process keeps the integrity of SR material reliability. Therefore, the process can be a beneficial tool that provides an additional dimension to SR structures without compromising SR material performance. Unique SR structures can be formed by applying the RT process, such as multi-step structures and half-etched SR structures that are beneficial for ultra-thin packaging, high density packaging, and multi-chip module packaging.

REFERENCES

- [1] A. Yoshida et al., "A study on package stacking process for package-on-package (PoP)," 56th Electronic Components and Technology Conference 2006, San Diego, CA, USA, 2006, pp. 6 pp.-, doi: 10.1109/ECTC.2006.1645753.
- [2] C. Cognetti, "Evolution of Semiconductor Packaging. Present and Future," EuroSime 2006 - 7th International Conference on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems, Como, Italy, 2006, pp. 1-1, doi: 10.1109/ESIME.2006.1644056.
- [3] M. -C. Hsieh, S. Lin, I. Hsu, C. -Y. Chen and N. Cho, "Fine pitch high bandwidth flip chip package-on-package development," 2017 21st European Microelectronics and Packaging Conference (EMPC) & Exhibition, Warsaw, Poland, 2017, pp. 1-5, doi: 10.23919/EMPC.2017.8346847.
- [4] W. W. -M. Dai, "Historical Perspective of System in Package (SiP)," in IEEE Circuits and Systems Magazine, vol. 16, no. 2, pp. 50-61, Secondquarter 2016, doi: 10.1109/MCAS.2016.2549949.
- [5] C. C. Chao, K. H. Chen, R. Kaw, J. Leibovitz, V. K. Nagesh and K. D. Scholz, "Multi-chip packaging for high performance systems," Proceedings 1988 IEEE International Conference on Computer Design: VLSI, Rye Brook, NY, USA, 1988, pp. 76-81, doi: 10.1109/ICCD.1988.25663.
- [6] R. W. Harcourt, D. Lovell, J. S. Rogers and S. D. Wadsworth, "The use of multichip module technology in system miniaturisation," IEE Colloquium on Advances in Interconnection Technology, London, UK, 1991, pp. 7/1-7/3.
- [7] R. R. Tummala, "SOP: what is it and why? A new microsystem-integration technology paradigm-Moore's law for system integration of miniaturized convergent systems of the next decade," in IEEE Transactions on Advanced Packaging, vol. 27, no. 2, pp. 241-249, May 2004, doi: 10.1109/TADVP.2004.830354.
- [8] M. Shevelov et al., "Small form factor and low profile quad-band System-in-Package (SiP) module," 2011 IEEE MTT-S International Microwave Symposium, Baltimore, MD, 2011, pp. 1-4, doi: 10.1109/MWSYM.2011.5972704.
- [9] S. S. Iyer, "Heterogeneous Integration for Performance and Scaling," in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 6, no. 7, pp. 973-982, July 2016, doi: 10.1109/TCPMT.2015.2511626.
- [10] S. Shimada, K. Okada, T. Kudo, C. Ueta and Y. Suzuki, "High Reliability Solder Resist with Strong Adhesion and High Resolution for High Density Packaging," 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, USA, 2019, pp. 1015-1021, doi: 10.1109/ECTC.2019.00159.
- [11] K. Okada and T. Shiina, "Development of photosensitive solder resist with high reliability for semiconductor package," 2015 IEEE 65th Electronic Components and Technology Conference (ECTC), San Diego, CA, 2015, pp. 367-372, doi: 10.1109/ECTC.2015.7159619.
- [12] Y. Suzuki and Y. Toyoda, "Selective Thinning Technology of Solder Resist for Ultra-Thin and High-Density IC Packaging," 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2021, pp. 774-780, doi: 10.1109/ECTC32696.2021.00133.
- [13] D. Whitehouse, "Surfaces and their Measurement" Gulf Professional Publishing, 2004.