A Novel Indium Metal Thermal Interface Material and Package Design Configuration to Enhance High-Power Advanced Si Packages Thermal Performance

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Abstract—High performance computing (HPC) flip chip packages provide powerful computing to solve complex problems in science, engineering, and business applications. High-performance flip chip package is built with advanced Si nodes, which may include multi-dice system to achieve great performance. Its market also grows significantly in recent years. These flip chip packages could generate more than 1000W power consumption. Thus, development of new thermal interface material (TIM) to enhance thermal performance of high-performance flip chip package is a key focus area. An indium metal with high thermal conductivity (81 W/mK) is used to demonstrate end-of-line thermal performance for advanced Si packaging with high power consumption.

The thermal resistance theta-JC (Rjc) is the key parameter while evaluating the thermal performance of lidded flip chip package as well as to validate TIM material characterization and package design configuration. In this study, a thermal test chip is designed and assembled into lidded flip chip package, and indium metal TIM is applied for thermal performance validations. A plunger with pneumatic cylinder and chiller water-cooling system is applied for lidded flip chip package thermal performance Rjc measurement. This work is to validate indium metal TIM thermal performance for lidded flip chip package with high power (1000 watts above) dissipation through Rjc thermal measurement. A computational fluid dynamics (CFD) modeling method was conducted using electronics cooling simulation software FloTHERM® to study the indium metal TIM integrated with package design guidance for lidded flip chip packaging. Modeling results were calibrated with experimental thermal test chip junction temperature (Tj) and package thermal performance Rjc measurements. Based on collected modeling and measurement data, it was revealed that indium metal TIM is capable of dissipating 1000 watts power consumption and still maintains maximum chip junction temperature at 105°C.

The proposed methodology in this paper has been validated and package design guideline for indium metal TIM application to meet package with high power thermal performance requirements will be proposed upon the findings of this study, which product / package designers can benefit from the superior devices and advanced packaging.

Keywords: High performance computing (HPC) flip chip package, indium metal thermal interface material, thermal resistance theta-JC, plunger with water cooling system, computational thermal modeling technique method, high power dissipation, and junction temperature

I. INTRODUCTION

Flip chip packaging technology has been introduced for many years to address the needs in the electronic packaging industry, which can provide better density and performance trade-off packaging solution. Increased functionality and performance requirements from the demands of electronics industry to solve complex problems in science, engineering, or business are pushing high performance computing (HPC) flip chip packaging development. The thermal requirements of flip chip packaging depend upon the amount of power dissipation in Si devices during operation. High performance flip chip package may create more than 1000 watts power consumption for high I/O microprocessor devices with large silicon chip size [1-2], which advanced thermal management may be needed to resolve thermal related challenges. Fig 1. shows a typical cross-sectional schematic of high-performance flip chip ball grid array (HFCBGA) package with the heat spreader that uses thermal interface material (TIM) to dissipate heat through the backside of die to the heat spreader [3-4]. The heat spreader is attached on the substrate using the stiffener with top and bottom adhesives. The heat dissipation performance of HFCBGA package highly depends on the ability of TIM to transfer heat efficiently from the backside of die to the heat spreader.

Figure 1. Schematic of high-performance flip chip ball grid array (HFCBGA) package configuration and heat flow paths.
Typically, thermal interface materials (TIMs) including thermal greases, thermal films, conductive pastes, and phase change materials (PCMs), are used as the interface between the die and the heat spreader [5-7]. To address the thermal performance requirements for high-power lidded flip chip package design, many semiconductor adhesive suppliers are developing new thermal interface materials with high thermal conductivity such as graphite and metal TIMs [8-11] (see Fig. 2) to fulfill high power consumption demands in high-performance flip chip packages. Herein, indium metal TIM with high thermal conductivity around 81 W/mK is introduced for next generation microprocessor (CPU) instead of polymer TIM, which is more efficiency of thermal conduction performance than polymer TIM for advanced high-performance computing flip chip package with high power consumption. Some literatures had investigated polymer or gel type TIMs thermal performance for a lidded flip chip package with low power consumption (100 watts and below) [12-14]. This paper is to study indium metal TIM thermal performance and package design configuration for high-performance lidded flip chip package with high power (1000 watts) dissipation through thermal performance measurement and modeling technique method assessment.

![Graphite-TIM and Metal-TIM](image1)

**Figure 2.** Thermal interface material (TIM) application for power consumption requirement.

Usually, the thermal resistance theta-JC, Rjc is used as the key parameter to estimate the heat dissipation capability of Si packaging [15-16]. Thermal resistance Rjc is the resistance of Si packaging to heat dissipation and is inversely related to the thermal conductivity of Si packaging. Thermal test chips are commonly used as a test vehicle to determine the thermal resistance Rjc. The thermal test chip usually includes two main functions: heater unit to provide heating power and thermal sensor to detect the chip temperature. In this study, a thermal test chip is designed and assembled into lidded flip chip package, and indium metal TIM is applied for thermal performance validations. A plunger with pneumatic cylinder and chiller water-cooling system is used for lidded flip chip package thermal resistance Rjc measurement (see Fig. 3). A powerful cooling head with chiller temperature 25°C is used for thermal test chip cooling. The case temperature (Tc) is measured by thermocouple placed at the heat spreader center. The data acquisition (DAQ) tool is used to measure the test chip junction temperature (Tj). The thermal resistance Rjc is calculated from (Tj - Tc) / heating power. A thermal modeling temperature distribution analysis were conducted to evaluate the heat dissipation capability of indium metal TIM and package design guideline for lidded flip chip package. Moreover, the appropriateness of thermal models is demonstrated by comparing the predicted thermal test chip junction temperature (Tj) and package thermal resistance Rjc with experimental results measured by DAQ tool.

![Thermal test chip design](image2)

**II. THERMAL TEST CHIP DESIGN**

To validate the indium metal TIM thermal performance and the accuracy of developed thermal modeling technique method, a thermal test chip with size 25.6 x 27 mm² (690 mm²) is designed, which contains 144 heater units to heat up the chip and 13 thermal sensors to sense the temperature, shown in Fig. 4. All heater units and thermal sensors are designed in the copper metal layer trace of chip to meet the target size and resistance, shown in Fig. 5. The 4-points resistance temperature detector (RTD) sensor are used as thermal die sensors for the measurement of test chip junction temperature. For the designed thermal test chip in this study, 13 thermal sensors located at chip corners (S1, S3, S11, S13), chip edges (S2, S6, S8, S12), chip mid (S4,
S5, S9, S10), and chip center (S7). To meet the high power (1000 watts) requirement in the designed thermal test chip for this research, the 144 heater units are divided into 16 1st-level heater groups (group A ~ group P), and heater units are connected in PCB. Each heater group includes 9 heater units connected in parallel, shown in Fig. 6. The 16 1st-level heater groups are further divided into 4 2nd-level heater groups (groups W, X, Y, Z) as shown in Fig. 7. The 2nd-level heater group includes 4 1st-level heater group connected in parallel and the 4 2nd-level heater groups are connected in series.

Figure 4. Schematic of heater unit and thermal sensor location in designed thermal test chip.

Figure 5. Target size and resistance for heater unit and thermal sensor.

Figure 6. Schematic of heater unit grouping configuration.

III. THERMAL MEASUREMENT SETTING AND MODELING CALIBRATION

A. Thermal Test Chip Design and Thermal Measurement

In this study, the designed thermal test chip with 25.6 x 27 mm² size is assembled into lidded flip chip package with 65 x 65 mm² size, and indium metal TIM1 is applied for thermal characterization measurement. In indium metal TIM1 assembly process, the bottom surface of heat spreader and the top surface of die in contact with indium metal TIM1 have the gold plating to enhance soldering quality, and a 350 μm thickness indium metal TIM1 is placed on the top surface of die with the soldering flux dispensed. The heat spreader is then attached on the stiffener (with top adhesive) and indium metal TIM1, and a snap pre-cure is performed for adhesive curing. Finally, the indium metal TIM1 is reflowed with 257°C peak temperature oven cure.

A powerful cold plate is used for device under test (DUT) cooling. A thermal pad with thermal conductivity 2 W/mK and thickness 0.5 mm is used as TIM2 between the cold plate and the DUT for a lidded flip chip package, and the DUT is put in the socket placed on the PCB as shown in Fig. 8. The heater headers of PCB are connected to power supply for power input and the sensor headers of PCB are connected to DAQ tool for thermal sensor temperature measurement. Thermocouple is placed on the top surface center of heat spreader to measure the case temperature (Tc). To inherently maintain the good contact between the thermocouple tip and the heat spreader surface, a thermocouple with the diameter 80 μm is used and the thermocouple pin is attached closely on the top surface of heat spreader under the plunger pressure force 75 kg applied on the thermal pad TIM2.

The RTD (Resistance Temperature Detector) sensor calibration is a must before having any action of thermal measurement. For thermal test chip design in this study, The RTD thermal sensor uses copper trace to achieve designed electrical resistance and copper has linear relationship between the electrical resistance and the temperature. The RTD relation equation between the thermal sensor electrical resistance and the temperature can be formulated as Resistance = M x Temperature + N, where M is the slope.
and $N$ is the intercept constant. To calibrate $M$ and $N$ values for the RTD equation using linear regression, the thermal sensor resistance is recorded at 10 different temperatures ranging from 40°C to 80°C, shown in Fig. 9. With the calibrated RTD equation, the junction temperature ($T_j$) can be obtained for the measured thermal sensor resistance. The steady state $T_c$ and $T_j$ temperatures are measured and used for thermal model calibration and the package thermal resistance $R_{jc}$ can be obtained from $(T_j - T_c) / \text{power}$. The heating power of the thermal test chip for thermal modeling calibration is set at 400 watts.

### B. Thermal Modeling Calibration

A three-dimensional (3-D) computational fluid dynamics (CFD) model is constructed using electronics cooling simulation software FloTHERM® which is a powerful commercial CFD tool [17], to perform the electrical packaging product thermal characterization analysis. The package considered in this present work is a high-performance flip chip ball grid array (HFCBGA) package with 3968 I/Os in an area-arrayed format. The die size of the flip chip package is $25.6 \times 27 \text{ mm}^2$ with a thickness of 755 μm (29 mils). The size of substrate is $65 \times 65 \text{ mm}^2$, and it has a thickness of 1452 μm. The three-dimensional thermal characterization model includes the full model of HFCBGA package with the heat spreader, PCB, and the cold-plate cooling module. Figure 10 displays (a) full thermal characterization model configuration and (b) cross-sectional mesh structure.

![Figure 8. Thermal characterization measurement setup for (a) cooling the package put on socket using cold plate and (b) PCB design with heater and sensor headers.](image)

![Figure 9. RTD sensor calibration for different temperatures.](image)

The package dimensions and thermal conductivities are listed in TABLE I. To mimic the real situation, the thermal contact resistance for TIM1 with 0.00926 °C/W and TIM2 with 0.0071 °C/W are included in the thermal characterization model. Because the silicon die thermal conductivity is sensitive to the temperature ($T$), a temperature dependent thermal conductivity for die is used. The substrate thermal conductivity is set based on copper density with orthotropic thermal conductivity. Each heater unit power is set to 2.78 watts to provide 400 watts uniform heating, and the cold plate with the cooling water
temperature 25°C is used for the thermal characterization model calibration with the measured junction temperature (Tj) of thermal test chip, the case temperature (Tc) of heat spreader, and the thermal resistance (Rjc) of package.

The modeling prediction maximum junction temperature (max. Tj), the case temperature (Tc), and the thermal resistance (Rjc) shows the same trend with experimental results, differences between modeling and experimental results are listed in TABLE II. The max. Tj and Tc temperature differences between the experiment and modeling is less than 1°C. The Rjc is calculated from (max. Tj - Tc) / 400 watts and its difference between the experiment and modeling is less than 0.001°C/W. Figure 11 displays the modeling junction temperature results compared to experimental data for all 13 thermal sensors. The thermal modeling shows the good match with experiment results of junction temperature after calibration, and considered with the measurement resolution of experiment tool, the modeling accuracy was reasonable as well. This modeling methodology will be used for the following investigation.

TABLE I. Package dimensions and thermal conductivities.

<table>
<thead>
<tr>
<th>Component</th>
<th>Size (mm)</th>
<th>Thickness (mm)</th>
<th>Thermal conductivity (W/mK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die</td>
<td>25.6 x 27</td>
<td>0.755</td>
<td>117.5 - 0.42 x (T - 100)</td>
</tr>
<tr>
<td>Substrate</td>
<td>65 x 65</td>
<td>1.452</td>
<td>Plane: 46.5 Normal: 0.34</td>
</tr>
<tr>
<td>Top adhesive</td>
<td>6.5mm wide</td>
<td>0.0825</td>
<td>1.2</td>
</tr>
<tr>
<td>Bottom adhesive</td>
<td>6.5mm wide</td>
<td>0.0825</td>
<td>1.2</td>
</tr>
<tr>
<td>Stiffener</td>
<td>6.5mm wide</td>
<td>1.0</td>
<td>14.9</td>
</tr>
<tr>
<td>Heat spreader</td>
<td>65 x 65</td>
<td>2.5</td>
<td>385</td>
</tr>
<tr>
<td>Underfill</td>
<td>25.6 x 27</td>
<td>0.815</td>
<td>1.0</td>
</tr>
<tr>
<td>TIM1</td>
<td>25.6 x 27</td>
<td>0.35</td>
<td>81</td>
</tr>
<tr>
<td>TIM2</td>
<td>65 x 65</td>
<td>0.5</td>
<td>2.0</td>
</tr>
</tbody>
</table>

TABLE II. Thermal characterization differences between modeling and experimental results.

<table>
<thead>
<tr>
<th>Thermal characterization</th>
<th>Maximum junction temperature (max. Tj) (°C)</th>
<th>Case temperature (Tc) (°C)</th>
<th>Thermal resistance (Rjc) (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modeling</td>
<td>106.2</td>
<td>96.8</td>
<td>0.023</td>
</tr>
<tr>
<td>Experiment</td>
<td>106.0</td>
<td>96.7</td>
<td>0.023</td>
</tr>
<tr>
<td>Difference</td>
<td>0.2</td>
<td>0.1</td>
<td>&lt; 0.001</td>
</tr>
</tbody>
</table>

IV. RESULTS AND DISCUSSIONS

A. TIM2 Thermal Conductivity Effect

Two types of commercial TIM2 including the thermal pad and thermal grease are considered in the thermal model to approach the power input to 1,000 watts with the maximum junction temperature ranging from 100°C to 105°C. Different levels of effective thermal conductivity with the contact resistance effect for the thermal pad and thermal grease is listed in TABLE III, which applied in this thermal model to investigate the maximum achievable power input. The chiller temperature is decreased to 15°C to gain more power input.

Figure 12 shows the maximum achievable power input for the thermal grease and thermal pad applications with the maximum junction temperature at 100°C ~ 105°C. For thermal pad application, although the thermal conductivity is increased to 25 W/mK the maximum power input only reaches ~870 watts to keep the maximum junction temperature at 100°C ~ 105°C due to the thicker thermal pad with 500 μm, which is a common value for the thermal pad with high thermal conductivity. For thermal grease application, the thickness is usually much lower than thermal pad (20 μm setting in this thermal model), and thus higher power input can be achieved as compared to thermal pad cases as shown in the Fig. 12, even with lower thermal conductivity ranging from 1.9 W/mK to 8.3 W/mK. In the following investigation, the thermal grease with thermal conductivity 8.3 W/mK is selected and the maximum power input is 1,008 watts with the maximum junction temperature at ~104°C to study indium metal TIM thermal performance and package design configuration.

TABLE III. TIM2 conditions applied in the thermal model.

<table>
<thead>
<tr>
<th>TIM2 type</th>
<th>Thickness (μm)</th>
<th>Effective thermal conductivity with contact resistance effect (W/mK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal pad</td>
<td>500</td>
<td>5, 9, 12.5, 17.8, 25</td>
</tr>
<tr>
<td>Thermal grease</td>
<td>20</td>
<td>1.9, 5, 6, 7, 8.3</td>
</tr>
</tbody>
</table>
Figure 12. TIM2 thermal conductivity effect on maximum achievable power input.

B. TIM1 Thickness Effect

In the HFCBGA package, TIM1 is inserted between the heat spreader and silicon die to enhance the thermal coupling between them. Most of the heat flux is transferred from the die through the TIM1 to the top of the package for cooling. Thus, the selection of TIM1 has a great impact on the thermal performance of the entire packaging. The thermal resistance \( R \) is proportional to the material thickness \( L \) and inversely proportional to the material conductivity \( K \) and contact area \( A \) \[18\].

\[
R = \frac{L}{KA}, \quad R_{jc} = R_{\text{heat spreader}} + R_{\text{TIM}} + R_{\text{Die}}
\]

From the numerical simulation about TIM1 thickness effect on the thermal performance, shown in Fig. 13. The \( R_{jc} \) performance is proportional to the TIM1 thickness. Thinner TIM1 can enhance the thermal performance with lower thermal resistance \( R_{jc} \) and thus lower the junction temperature of the die. When TIM1 thickness is decreased from 350 \( \mu m \) to 30 \( \mu m \), the thermal performance can be enhanced by \(-22\%\).

C. Die Thickness Effect

In this section, the thermal behavior with the die thickness ranging from 380 \( \mu m \) to 755 \( \mu m \) is investigated. To maintain the same package form factor, the metal indium TIM1 thickness is increased to meet the gap between the die and the heat spreader structure when the die thickness is decreased. The results shown in Fig. 14, which indicate that \( R_{jc} \) value raises about 4\% from 0.027 \( ^\circ C/W \) to 0.028 \( ^\circ C/W \) when the die thickness is decreased from 755 \( \mu m \) to 380 \( \mu m \). Due to the high thermal conductivity of indium metal TIM1 (81 W/mK setting in the thermal model), the compensation with indium metal TIM1 for the lack of the highly conductive silicon die has slight impact on the package \( R_{jc} \) performance with decreasing the die thickness from 755 \( \mu m \) to 380 \( \mu m \). If a polymer TIM1 with a lower thermal conductivity, such as 3 W/mK, is selected for the package, the \( R_{jc} \) performance impact with decreasing the die thickness will be more sensitive.

Consequently, for the package with a thinner die, the TIM1 selection with high thermal conductivity will be necessary to fulfill the package with high power thermal performance requirements.

D. Substrate Thickness Effect

In a test environment with good cooling capacity cold plate at the top, 99.7\% of heat will be dissipated from the top through the heat spreader and only 0.3\% of the heat will be dissipated from the bottom through the substrate \[4\]. From the simulation results as shown in Fig. 15, when the thickness of the substrate is reduced from 1452 \( \mu m \) to 202 \( \mu m \), the \( R_{jc} \) performance of the package keeps stable, while the junction temperature \( T_j \) rises slightly. The reason is that it is difficult to dissipate the heat from the bottom of package, so the thicker substrate will enhance the transverse heat conduction, and the heat is then picked up by the stiffener. The efficiency of heat dissipation, however, is very minor. Thus, the thickness of the substrate has insignificant influence on the overall thermal characteristics of the package.
E. Heat Spreader Thickness Effect

The heat spreader structure of a lidded flip chip package type is the major heat flow path to spread out the heat generated by Si die to the ambient cooling system which is affixed to the top surface of the heat spreader structure. As power dissipation increases, a good thermal solution to improve the package thermal performance is essential. Therefore, it is worthwhile to investigate the heat spreader geometry on the package thermal performance.

This section focuses on the heat spreader thickness dimension ranging from 1 mm to 2.5 mm while the other package geometry and power input are fixed. The simulation results as shown in Fig. 16 indicate that the package thermal performance $R_{jc}$ is linearly decreased from 0.027 °C/W to 0.022 °C/W (down 18.5%), the silicon die junction temperature $T_j$ keeps stable, while the heat spreader temperature $T_c$ increases from 77.7°C to 82.3°C when the heat spreader thickness is decreased from 2.5 mm to 1 mm. For a thicker heat spreader, more heat flow can be spread out from the heat spreader center hot-zone region to the heat spreader perimeter region, which lowers down the heat spreader temperature ($T_c$) and results in a higher $R_{jc}$ value.

F. Die Size Effect

In this section, the thermal behavior with the die size ranging from 691 mm$^2$ to 165 mm$^2$ is investigated with keeping maximum power 1,008 watts input. The results shown in Fig. 17 indicate that the smaller die size (165 mm$^2$) with high power consumption 1,008 watts will generate very high junction temperature 235°C ($R_{jc}$ performance = 0.117 °C/W), even using the higher thermal conductivity indium metal TIM1. To meet the maximum junction temperature below than 105°C with the die size reduced, the maximum allowable power must be down-graded for the smaller die size application to prevent silicon device burn-out issues. A reference maximum allowable power for different die sizes with maximum junction temperature fixed at 105°C is listed in TABLE IV.

![Figure 15](image)

**Figure 15. Substrate thickness effect on the thermal performance.**

![Figure 16](image)

**Figure 16. Heat spreader thickness effect on the thermal performance.**

![Figure 17](image)

**Figure 17. Die size effect on the thermal performance with maximum power fixed.**

**TABLE IV. Maximum allowable power for different die sizes with maximum junction temperature fixed at 105°C.**

<table>
<thead>
<tr>
<th>Die size (mm$^2$)</th>
<th>691</th>
<th>476</th>
<th>300</th>
<th>165</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum junction temperature (°C)</td>
<td>104.5</td>
<td>104.3</td>
<td>104.3</td>
<td>104.4</td>
</tr>
<tr>
<td>Maximum allowable power (watt)</td>
<td>1,008</td>
<td>824</td>
<td>570</td>
<td>441</td>
</tr>
</tbody>
</table>

V. CONCLUSIONS

This research in present work examines the indium metal TIM thermal performance on high-performance flip chip packaging with high power consumption. An in-house thermal test chip is designed and assembled into a high-performance flip chip ball grid array (HFCBGA) package with two-piece heat spreader structure. A plunger with pneumatic cylinder and chiller water-cooling system is designed and used for the silicon die junction temperature and full package thermal resistance $R_{jc}$ measurement. A three-dimensional (3-D) computational fluid dynamics (CFD) modeling technique method is used to simulate the thermal characterization of indium metal TIM.

The following conclusions can be drawn based on the
analyzed results. Firstly, the proposed and calibrated methodology in this paper is based on a designed thermal test chip and assembled into a package test vehicle with known die, substrate, stiffener, adhesive, underfill, heat spreader designs and material properties. Modeling indicated the indium metal TIM is capable of dissipating 1000 watts power and maintains a maximum junction temperature at 105°C using the thermal grease TIM2 with thermal conductivity 8.3 W/mK. In addition, to meet the maximum junction temperature lower than 105°C for small die size design, the maximum allowable power consumption for different die sizes is also provided. Finally, the findings of this study can offer some design suggestions while using indium metal TIM in advanced Si packaging.

REFERENCES


