FORMS: Fine-grained Polarized ReRAM-based In-situ Computation for Mixed-signal DNN Accelerator

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Abstract—Recent work demonstrated the promise of using resistive random access memory (ReRAM) as an emerging technology to perform inherently parallel analog domain in-situ matrix-vector multiplication—the intensive and key computation in deep neural networks (DNNs). One key problem is the weights that are signed values. However, in a ReRAM crossbar, weights are stored as conductance of the crossbar cells, and the in-situ computation assumes all cells on each crossbar column are of the same sign. The current architectures either use two ReRAM crossbars for positive and negative weights (PRIME), or add an offset to weights so that all values become positive (ISAAC). Neither solution is ideal: they either double the cost of crossbars, or incur extra offset circuitry. To better address this problem, we propose FORMS, a fine-grained ReRAM-based DNN accelerator with algorithm/hardware co-design. Instead of trying to represent the positive/negative weights, our key design principle is to enforce exactly what is assumed in the in-situ computation—ensuring that all weights in the same column of a crossbar have the same sign. It naturally avoids the cost of an additional crossbar. Such polarized weights can be nicely generated using alternating direction method of multipliers (ADMM) regularized optimization during the DNN training, which can exactly enforce certain patterns in DNN weights. To achieve high accuracy, we divide the crossbar into logical sub-arrays and only enforce this property within the fine-grained sub-array columns. Crucially, the small sub-arrays provide a unique opportunity for input zero-skipping, which can significantly avoid unnecessary computations and reduce computation time. At the same time, it also makes the hardware much easier to implement and is less susceptible to non-idealities and noise than coarse-grained architectures. Putting it all together, with the same optimized DNN models, FORMS achieves 1.50× and 1.93× throughput improvement in terms of $\frac{\text{TOPS}}{W}$ and $\frac{\text{TOPS}}{W^2}$ compared to ISAAC, and 1.12× $\sim$ 2.4× speed up in terms of frame per second over optimized ISAAC with almost the same power/area cost. Interestingly, FORMS optimization framework can even speed up the original ISAAC from 10.7× up to 377.9×, reflecting the importance of software/hardware co-design optimizations.

I. INTRODUCTION

Deep Neural Networks (DNNs) have become the fundamental element and core enabler of ubiquitous artificial intelligence, thanks to their high accuracy, excellent scalability, and self-adaptiveness [1]. As the ever-growing DNN model size, the high computation and memory storage of DNN models introduce substantial data movements, posing key challenges to the conventional Von Neumann architectures, where weight storage and computation units are separate. To reduce data movement, many compression techniques [2–4] and hardware accelerators [5–11] have been intensively investigated. However, as Moore’s law is reaching an end [12], the potential of the acceleration architecture based on conventional technology is still limited. We argue that drastic improvements can be only achieved by 1) the next-generation emerging device/circuit technology beyond CMOS; and 2) the vertical integration [13] and optimization of algorithm, architecture, and technology innovations to deliver better overall performance and energy efficiency for various applications.

A promising emerging technology is the recently discovered resistive random access memory (ReRAM) [14, 15] devices that are able to perform the inherently parallel in-situ matrix-vector multiplication in the analog domain. This key feature has been applied to several significant problems, including solving systems of linear equations in $O(1)$ time complexity [16], and more interestingly, building DNN accelerators [17–24]. Since the key computation in DNNs can be essentially expressed as matrix-vector multiplication, ReRAM crossbars can naturally accelerate DNNs with much less data movement and low-cost computation. Due to their promising results, structured pruning [3] and quantization [4] are also developed to facilitate a smaller number of weights and bits to reduce the amount of computation and ReRAM hardware resources.

On the other side, a key complication of the ReRAM-based DNN accelerator is that although the weights stored in ReRAM crossbar cells can be either positive or negative, the in-situ computation assumes all cells in each crossbar column hold values of the same sign, i.e., all positive or all negative. There are two approaches to tackle the problem. The general way is to use two ReRAM crossbars to hold the positive and negative magnitudes weights separately, doubling the ReRAM portion of hardware cost [17–19]. In contrast, ISAAC [18] adds an offset to weights so that all values become positive. While keeping the number of crossbars the same, the latter approach introduces additional hardware costs for the peripheral circuits by adding extra offset circuitry and may also decrease the network robustness to hardware failures [20]. We argue that both solutions are not ideal, and we attempt to develop an alternative approach with better cost/performance...
Different from the previous approaches, which use additional hardware to “fix” the problem, our design principle is to enforce exactly what is assumed in the in-situ computation—ensuring the pattern that all weights in the same column of a crossbar have the same sign. This idea takes the opportunity of algorithm and hardware co-design, and is motivated by the capability of the powerful alternating direction method of multipliers (ADMM) regularized optimization [30], which is exactly able to enforce patterns in DNN training while maintaining high accuracy. Based on this idea, we can train a DNN model using ADMM with our novel constraints such that the weights mapped to the same crossbar columns are all positive or negative. With the typical ReRAM crossbar size, e.g., $128 \times 128$, we found that the “same-sign” property of the coarse granularity, i.e., the whole column of 128 weights, can lead to accuracy degradation. To maintain high accuracy, we propose to divide the crossbar into smaller logical sub-arrays and only enforce the property within the fine-grained sub-array columns, and use fine-grained computation instead of coarse-grained computation (i.e., calculate fine-grained sub-array column at each time). However, this raises another problem: the mainstream designs take advantage of coarse-grained computation to achieve high performance (i.e., frames per second (FPS)). For a fine-grained design to reach a similar FPS to that of coarse-grained designs, if no other optimizations are applied, more parallel analog-to-digital converters (ADCs) are needed to operate in parallel to compensate for the performance degradation caused by computation granularity, which will generally lead to a higher hardware overhead than the coarse-grained designs.

Is this yet another failed idea that seems to work at the first thought but actually not after deliberation? Fortunately, the answer is no, because our idea opens a new opportunity for more significant performance improvements. The crucial observation is that if all inputs to the crossbar become zeros in higher bits after a certain position, e.g., $000001011$, they can be simply skipped, saving cycles and improving performance. The effectiveness of the input zero-skipping technique is determined by the size of the crossbar sub-array. The smaller the number of inputs, the higher the probability all inputs become zero at the higher bits, thereby more zeros can be skipped. This is why zero-skipping is a unique opportunity for small sub-arrays. With a fraction of a crossbar column (e.g., 4 or 8 cells), zeros can be aggressively skipped among 4 or 8 inputs. Moreover, it is worth noting that small ADCs for fine-grained computation are easier to implement than large ADCs for coarse-grained computation, and make the design less susceptible to non-idealities and noise [31, 32].

Putting all together, this paper proposes FORMS, the first algorithm/hardware co-designed fine-grained ReRAM architecture solution leveraging polarized weights. The overall flow of FORMS algorithm/hardware co-design is shown in Figure 1. Starting with a pretrained model, we first apply structured pruning. Then, the weight matrix in the pruned model is divided into fixed-sized fragments, and each fragment corresponds to a column of the crossbar sub-array. By incorporating our fragment polarization constraints in ADMM regularized training, the weights in each fragment will be trained to have the same sign. Please note that we are not moving the weights around to form polarized fragments. Finally, the quantization is applied to reduce the number of bits required for each weight. With the multi-step ADMM-based structured pruning, polarization, and quantization, a significant model compression ratio is achieved.

At the hardware level, we design a fine-grained DNN accelerator architecture leveraging fine-grained computations. A novel zero-skipping logic is developed to control the shift of input bit streams on-the-fly and avoids entering the unnecessary zero bits into each layer of the DNNs-based ReRAMs to eliminate useless computations and start computation on the next input early. Applied to the inputs of a small sub-array (fragment), zero-skipping significantly reduces the frame processing time and energy consumption.

### II. BACKGROUND AND CHALLENGES

#### A. ReRAM Crossbar and ReRAM-Based DNN Acceleration

Recently, there is significant progress in fabricating non-volatile memories. The 3D Xpoint [33, 34] is an example of commercial non-volatile memories fabricated jointly by Micron and Intel. Resistive RAM is a non-volatile memory with nearly zero leakage power, high integration density, and high scalability. Research papers demonstrated the results of fabricated ReRAM memory cells, memory arrays [35] and also neuromorphic accelerators using ReRAM technology [33, 50].

Several ReRAM-based in situ mixed signal DNN accelerators such as ISAAC [18], Newton [19], PipeLayer [20], PRIME [47], PUMA [45], MultiScale [22], XNOR-RRAM [57], RapidDNN [38], have been proposed in recent years. These designs utilize a combination of analog and digital units to speed up the computation. Besides, the recent work TIMELY [23] is proposed to enhance the analog data...
locality to keep computations in analog domain to save the energy cost of data movements and D/A and A/D domain conversion. The SRE [39] exploits the sparsity of both weights and activations to achieve better energy efficiency and performance by proposing hardware mechanisms. However, it induces remarkable hardware overhead as all mechanisms such as row indexing, routing controls, and word-line controls are hardware-managed. TinyADC [40] proposes a pruning solution that fixes the number of non-zero weights in each column of the ReRAM crossbar while their positions can vary. This helps to decrease the accumulated value and required ADC resolution. In contrast, FORMS proposes hardware-software co-design optimizations to improve frame processing rate, area, and power efficiency.

B. Challenges

Despite the recent research progress, we identify two challenges for ReRAM-based DNN acceleration.

Mapping signed weights. When we map the arbitrary DNN weights onto ReRAM crossbars, it is challenging to represent negative weights using positive conductance. Prior works address the problem differently. The general way is to decompose each weight into a positive magnitude portion and a negative magnitude portion, and use two crossbars to represent each of the portions [17, 26–28, 41]. This method doubles the hardware cost of the ReRAM crossbar. Instead, ISAAC [18] addresses this problem by shifting or adding an offset to the original negative weight value, so that all the weights become positive. To be able to calculate correct results, ISAAC needs to count the number of 1s in each individual input. If considering 16-bit weights are used, for each 1 in each input, a bias of $2^{15}$ must be subtracted from the final results. Counting all 1s for all inputs (that feed to the crossbar in parallel) and performing subtractions for each of 1s introduces significant overhead to ISAAC. Moreover, this mapping method decreases the network robustness to hardware failures [29]. We can see that both methods will cost extra resources in terms of area, power, and energy consumption.

ADC/DAC implementation. To ensure high throughput, the mainstream accelerator designs (e.g., ISAAC, PRIME, PUMA) take advantage of coarse-grained computations, a large number of ReRAM crossbar rows (e.g., 128 or 256) need to be processed at the same time and hence large ADCs are needed. However, the ADC does not scale as fast as the CMOS technology does [18, 42]. The recent study [40, 42] reports the ADC/DAC blocks may become the major contributor to the total chip area and power. To save power and area, many designs share an ADC with many crossbar columns (e.g., 128 columns in ISAAC). Therefore, the ADC needs to switch among those columns at a high-speed, which is hard in practice.

C. Motivation

We realize the possibility of generating polarized weights that can elegantly solve the natural problem of mapping positive/negative weights to the ReRAM crossbar without doubling crossbar cost or introducing extra hardware for result compensation. We explore a good balance between the overall hardware cost and performance. Even with paying the extra overhead to compensate for the performance degradation caused by fine-grained computation, our design can still achieve four benefits: 1) zero-skipping techniques can achieve significant performance improvements; 2) making ADC/DAC implementation less challenging compared to the state-of-the-art coarse-grained architecture designs (e.g., ISAAC, PUMA, and PRIME); 3) fine-grained architecture is less susceptible to non-idealities and noise than coarse-grained architecture; and 4) achieving a higher overall performance rate than coarse-grained designs under a similar power and area cost. We demonstrate that by leveraging the principle of algorithm and hardware co-design, our proposed solution significantly advances the state-of-the-art and paves a new way for fine-grained mixed-signal accelerators design.

III. HARDWARE-AWARE OPTIMIZATION FRAMEWORK

In this section, we describe the whole software procedure to generate hardware-friendly DNN models. The key novelty is the fragment polarization technique that enforces the same sign for weights in each fragment. As recent works [43–46] have demonstrated, the structured pruning and quantization are two essential steps for hardware-friendly model compression that are universally applicable to all DNN accelerators. Thus, we perform structured pruning before fragment polarization considering the size of the ReRAM crossbars, and quantization after. Thus, the sign of each fragment is determined by the structurally pruned model. And the quantization is applied after the structure and sign of the weights are determined. All of the three steps are uniformly supported by Alternating Direction Method of Multipliers (ADMM) regularized optimization method [50] which has shown to be very suitable for DNN training and produced state-of-the-art results [47]. In the following sections, we describe these three steps, and then explain how to express our desired pattern in ADMM.

A. Crossbar-Aware Structured Pruning

There are different types of structured sparsity in DNNs. FORMS combines two types of structured pruning methods—
filter pruning and filter-shape pruning. As shown in Figure 2, we reshape the weights from convolutional filters of a convolutional layer into a 2D weight matrix, each column represents all the weights from the same filter, while each row represents the weights on the same position of all filters. By adopting these two types of pruning, the entire columns and rows of the weight matrix will be removed while the remaining weight matrix is still dense. After the structured pruning, the weight matrix size becomes much smaller, which effectively reduces the number of ReRAM crossbars to store the weights and also removes the corresponding peripheral circuits.

The previous ReRAM-based accelerator designs [47, 48] apply structured pruning and aim to make the pruning ratio as high as possible while maintaining an acceptable accuracy loss. They do not take the ReRAM crossbar size into consideration, therefore causing performance degradation when the pruned model is mapped onto the ReRAM crossbars. For example, if the size of the crossbar is 128 × 128, only the portion of pruned columns/rows of weights that reaches the multiple of the 128 (e.g., 128, 256) will lead to the actual crossbar reduction. The remaining pruned columns/rows of weights still need to be stored as zeros on the crossbars. Consequently, those pruned columns/rows are wasted, and the accuracy drop is incurred without gaining the full benefit. In FORMS, we perform a crossbar-aware structured pruning by considering the crossbar size and carefully choosing the pruning ratio for each DNN layer to avoid unnecessary accuracy drop.

B. Fragment Polarization

A fragment is a set of consecutive weights mapped to ReRAM crossbar. The fragment size is determined by the number of rows in sub-array—a fragment contains weights that will be mapped to the same column of a sub-array, as shown in Figure 3. In our design, the weights in a fragment are polarized. They are either positive or negative. Therefore, the multiply-accumulate operations performed by each column of the ReRAM crossbar sub-array do not suffer from the arbitrary sign of its operands.

With the concept of fragment introduced, we need to consider two issues: 1) how to determine the sign of weights in a fragment; and 2) the mapping policy of weights to sub-array columns. The second problem matters because it determines which set of weights in the DNN model will contain the same sign. Next, we show how to handle these two problems.

To orchestrate fragment polarization during the training process, we calculate the sum of weights in each fragment and determine the fragment sign based on the following principle: if the sum is greater than or equal to 0, we set the sign of the fragment as positive, otherwise, we set it as negative. We incorporate ADMM regularized optimization with the fragment polarization constraint to regularize the weights to have the same sign as the fragment or to become zero. Eventually, the negative/positive weights are eliminated in positive/negative fragments.

During training, since the weights are continuously updated, the sign of a fragment changes. Specifically, at the beginning of fragment polarization, the fragment signs are determined by the above policy based on the structurally pruned model. Then, the training for fragment polarization starts. Let us assume that the training process contains $N$ epochs, each goes through the entire training dataset once. We can update the target sign every $M$ epochs. This means that at the end of $M$ epochs, the sign for each fragment will be calculated again using the current weights belonging of the fragment. During the training process, the fragment signs are updated for $N/M$ times.

Next, we consider the design space of mapping weights to fragments. As shown in Figure 3, given the weights of a convolution filter in 3-D format with width (W), height (H), and channel (C) dimension, we can naturally have three polarization policies. In width-major or W-major polarization, the consecutive weights in one or multiple consecutive rows in a filter are mapped to the same fragment. The weights in two consecutive fragments are also consecutive in the width-major order. After all weights in a filter are mapped, we move on to the next filter using the same procedure. More details regarding the ReRAM mapping scheme will be discussed in Section IV-A.

Similarly, we can define height-major or H-major polarization, and channel-major or C-major polarization. In particular, for C-major, the weights in the same position at all channels are mapped before moving to the next position of the filter.

Since the polarization policy determines which region of weights should have the same sign, different policies could affect accuracy. Our observation results show the W-major polarization scheme achieves the highest accuracy on the ImageNet dataset, where C-major polarization is the best choice for the CIFAR-10/100 dataset. Since the same polarization scheme will be applied over the entire neural network, we only need to uniformly re-order the weights with their corresponding inputs in advance, then directly map them to the ReRAM crossbars. Base on the chosen polarization scheme, the weights are trained to enforce the fragment polarization properties. There is no need to individually move the weights around to form a polarized fragment, and it will not incur any hardware overheads due to location indices.

C. ReRAM Customized Weight Quantization

We develop ReRAM customized weight quantization, to reduce the bit representation of weight parameters. Similar to crossbar-aware structured pruning, we consider the numbers of valid ReRAM conductance states into our quantization constraint during the training process. In reality, the number of ReRAM conductance states is limited by the provided resolution of the peripheral write and read circuitry. More state levels require more sophisticated peripheral circuitry. Due to limited computational accuracy, multiple ReRAM cells are usually used to represent one weight. For example, we need eight 2-bit ReRAM cells to represent one 16-bit weight, and four 2-bit ReRAM cells to represent one 8-bit weight. Thus,
the quantization can effectively reduce the design area and power consumption. In FORMS, if the 2-bit ReRAM cells are used in the design, the quantization bits will be set to the multiply of 2, which can fully utilize the resolution of the ReRAM cells. More importantly, compared to forcing a high-bit representation DNN model into a low-bit representation during the ReRAM mapping process, introducing the quantization to the training process allows the weights to be trained into a low-bit representation.

**D. ADMM Regularized Optimizations**

ADMM [30] is an advanced optimization technique, where an original optimization problem is decomposed into two subproblems that can be solved separately and iteratively. We incorporate ADMM-regularized training into FORMS training process to achieve and optimize the crossbar-aware structured pruning, fragment polarization, and ReRAM customized quantization feature. Using ADMM can guarantee the solution feasibility (satisfying ReRAM hardware constraints) while providing high solution quality (no obvious accuracy degradation after model compression and after hardware mapping).

Consider the $i$-th layer in an $N$-layer DNN, the weights and bias can be represented by $W_i$ and $b_i$. And we define the loss function as: $L({\{W_i\}}_{i=1}^{N}, {\{b_i\}}_{i=1}^{N})$. We minimize the loss function associated with DNN model and subject to the constraints of FORMS. Then the overall problem is given by:

$$\begin{align*}
\text{minimize} & \quad L({\{W_i\}}_{i=1}^{N}, {\{b_i\}}_{i=1}^{N}), \\
\text{subject to} & \quad W_i \in S_i, \quad W_i \in P_i, \quad W_i \in Q_i, \quad i = 1, \ldots, N, \tag{1}
\end{align*}$$

where $S_i$, $P_i$ and $Q_i$ are the constraint sets of Crossbar-aware Structured Pruning, Fragment Polarization and ReRAM Customized Quantization, respectively.

1) **Crossbar-aware Structured Pruning Constraints:**

In crossbar-aware structured pruning, we use $H$ to represent the weights in 2D format of a specific layer, as shown in Figure 2. The constraints in the $i$-th CONV layer becomes $W_i \in S_i := \{H | \text{the percentage of nonzero filters and filter-shapes in } H \text{ is less than or equal to } \alpha_i \text{ and } \beta_i, \text{ where } \alpha_i \text{ and } \beta_i \text{ are predefined hyperparameters. For example, suppose we want a 43% filter sparsity and 62% shape sparsity in } i\text{th layer, then we set } \alpha_i = 0.57 \text{ and } \beta_i = 0.38.\}$

2) **Fragment Polarization Constraints:**

For fragment polarization, the constraint set $P_i = \{\text{the weights on each fragment (a column of a crossbar sub-array) have the same sign}\}$, where the ReRAM crossbar sub-array size $m \times n$ is a predefined hyperparameter. The sign of the fragment is determined by the following function:

$$\text{Sign}_e = \begin{cases} 
+ & \text{if } \sum_{i=1}^{m} W_{ei} \geq 0, \\
- & \text{otherwise}, \end{cases} \tag{2}$$

where $i = 1, \ldots, m$ is the $i$-th weight on a fragment.

3) **Customized Quantization Constraints:**

For the ReRAM customized quantization, the set $Q_i = \{\text{the weights in the $i$-th layer are mapped to the quantization values}\}$. The quantization values depend on the characteristics of the ReRAM device such as conductance range and valid state levels.

**Fig. 4: Procedure of ADMM-Regularized Optimization.**

4) **ADMM-Regularized Optimization Flow:** As shown in Figure 4, the overall ADMM-regularized optimization flow is an iterative training process, which is similar in ADMM-NN [49]. Thanks to the flexibility in the definition of constraint sets $S_i$, $P_i$, and $Q_i$, the above constraints can be jointly included, or applied individually. First, we incorporate one of the three constraints by using indicator function, which is $g_i(W_i) = 0$ if $W_i \in S_i$ or $P_i$ or $Q_i$, otherwise.

Problem (1) with constraint cannot be directly solved by classic stochastic gradient descent (SGD) methods [50] as original DNN training. However, the ADMM regularization can reform and separate the problem, then solve them iteratively [51, 52]. First, we reformulate problem (1) as follows:

$$\begin{align*}
\text{minimize} \quad & f({\{W_i\}}_{i=1}^{N}, {\{b_i\}}_{i=1}^{N}) + \sum_{i=1}^{N} g_i(Z_i), \\
\text{subject to} \quad & W_i = Z_i, \quad i = 1, \ldots, N, \tag{3}
\end{align*}$$

where $Z_i$ is an auxiliary variable. With formation of augmented Lagrangian function, Problem (3) can be decomposed into two subproblems (4) and (5),

$$\begin{align*}
\text{minimize} \quad & f({\{W_i\}}_{i=1}^{N}, {\{b_i\}}_{i=1}^{N}) + \sum_{i=1}^{N} \rho_i \frac{1}{2} \|W_i - Z_i + U_i\|_F^2, \tag{4}
\end{align*}$$

$$\begin{align*}
\minimize_{\{Z_i\}} \quad & \sum_{i=1}^{N} g_i(Z_i) + \sum_{i=1}^{N} \frac{\rho_i}{2} \|W_i^{t+1} - Z_i + U_i\|_F^2, \tag{5}
\end{align*}$$

where $U_i$ denotes dual variable and $t$ is the iteration index. The positive scalars $\rho_i$ is a penalty hyperparameter for the $L2$ regularization. The first subproblem can be solved by classic SGD, and the solution for the second subproblem is given by

$$Z_i^{t+1} = \prod_{X_{\text{cross}}} (W_i^{t+1} + U_i), \tag{6}$$

where $\prod_{X_{\text{cross}}} (\cdot)$ is Euclidean projection to $X_i \in \{S_i, P_i, Q_i\}$, thereby weight matrices are structured pruned or fragment polarized or customized quantized. These two subproblems will be iteratively solved and we update $U_i$ in each iteration by $U_i^{t+1} := U_i^{t+1} + W_i^t - Z_i^t$ until convergence. The detailed solution process can refer to [54].

**IV. FORMS ARCHITECTURE**

This section describes the FORMS accelerator architecture that can execute the optimized DNN models generated by the FORMS optimization framework. Our design only needs to map the magnitude bits of all the weights to ReRAM crossbars without adding extra crossbars or offset circuits. To ensure high throughput, we develop a new pipelined design incorporated with zero skipping logic.
A. Mapping Scheme and Dataflow

In FORMS, instead of mapping both the sign and magnitude bits of arbitrary/mixed-signed weight values as in prior works such as memristive Boltzmann machine [55], ISAAC [18], Newton [19], PipleLayer [20], PRIME [17], PUMA [21], we only need to store the magnitude bits to the ReRAM, and the sign bit in each fragment in the 1R ReRAM-based array [56].

Figure 5 shows an example of the ReRAM mapping scheme on a crossbar array. We assume the physical crossbar array size is $q \times m$ rows by $p \times n$ columns (e.g., 128 by 128), where $q, p, m, n$ could be various depending on different design specifications. We partition the crossbar array into logical sub-arrays, where each sub-array has $m$ rows and $n$ columns. On one crossbar array, $q \times m$ weights from the same filter will be mapped on the same column, and the weights from different $p \times n$ filters will be mapped onto different columns of this crossbar array. The rest of the weights will be mapped onto other crossbar arrays in the same manner. Thus, in order to accommodate all the weights of a CONV layer, multiple ReRAM crossbar arrays are needed. In reality, due to the limitation of the ReRAM resolution, we need multiple ReRAM cells to represent one weight. For example, we need four 2-bit ReRAM cells to represent one 8-bit weight. In this way, each fragment will still have $m$ rows, but 4 columns instead of 1 column. And all $m$ weights in the same fragment that are represented by those $m \times 4$ ReRAM cells.

The optimized ReRAM-aware DNN model obtained from the ADMM regularized optimization process in Section III-D, has the fragment polarization property. Thus, all the weights within a fragment have the same sign, and we do not need to move the weights around to satisfy the polarization constraint. For each fragment, an associated 1R is used to store the sign bit. All the associated 1Rs are grouped as a sign indicator. The sign bits stored in the sign indicator will be carried out for accumulation in the digital domain.

Convolution Dataflow. CONV layers perform convolution of input feature maps and weight filters. The convolution results are then accumulated. After passing intermediate results through an activation function (e.g., rectified linear unit (ReLU)), we produce a single output feature map. By repeating this procedure for the rest of the weight filters, we obtain the whole output feature maps.

We fetch the digital inputs (feature maps) from eDRAM or DRAM (DRAM for input images, eDRAM for intermediate results) and arrange them into input buffers to be sent to DAC. The output of DAC becomes the analog input $v_i$ of the ReRAM crossbars. The matrix-vector multiplication can be performed by leveraging the feature of the ReRAM crossbars, and the output can be calculated by: $i_v = W^T v_i$. Each fragment (column) of the ReRAM crossbar sub-array produces an intermediate result, which is the accumulated current result. Intermediate results produced by all fragments will be propagated through ADC. The converted digital values will be carried to our proposed accumulation blocks along with the corresponding sign bits from sign indicator for accumulation.

The accumulation blocks are used for accumulating all the intermediate results from crossbar sub-arrays. The sign-bit indicator specifies whether the adder should work in add or subtract mode. The output of the adder will be accumulated to the temporary results from other fragments. Iteratively, we finish the CONV operation and obtain the output feature map to be stored into eDRAM, which will become the inputs (feature maps) of the next layer. By using the sign indicator with our polarized ReRAM crossbar mapping, our design can save half of the crossbars, which are used to store the positive/negative weights separately. When compared to the designs like ISAAC [18], FORMS avoids introducing the offset circuitry with small overhead caused by sign indicator. Moreover, since we only store the magnitude bits on ReRAM crossbars, FORMS can take the advantage to store one more magnitude bit when using the same number of ReRAM crossbars, which allows FORMS to achieve higher weight representation precision.

B. Fragment Size Exploration and Zero Skipping Logic

The fine-grained sub-array is a key feature of FORMS architecture that ensures high accuracy, more feasible hardware implementation, and significant performance improvement. We perform experiments to understand the relation between the size of fragment size and accuracy. Figure 6 shows that the smaller fragment size introduces zero or minor accuracy degradation in polarized form, while the larger fragment size may lead to a small accuracy degradation. Compared to the coarse-grained crossbars, the small fragment size corresponds to small ADCs. For example, FORMS can use 4-bit ADCs instead of one 8-bit ADC per each crossbar used in ISAAC [18] or PROMISE [57]. In general, the area and power of ADCs grow exponentially with the number of bits of ADCs. To save the area and power, ISAAC shares a large 8-bit ADC with 128 columns. Unfortunately, this leads to stringent hardware implementation requirement. Specifically, one 8-bit ADC must switch between 128 columns and convert the analog current to digital values within 100ns. This design makes ISAAC impractical for fabrication. More importantly, having fine-grained fragments opens a new opportunity to significantly improve performance by employing a novel zero skipping logic that reduces the required cycles to feed input bits to sub-arrays, leading to significant performance improvement.

To understand how FORMS saves input cycles, we use a 16-bit input representation as an example. For each clock cycle,
1 input bit is fed into the fragments in parallel. Generally, it needs 16 cycles to feed a 16-bit input to the crossbar. However, most inputs actually have small values [58] and can be represented by just a few bits, which means the upper bits are all 0s and can be skipped from feeding to the crossbar.

We define effective bits as the number of input bits that contribute to output results. It is obtained by removing the consecutive most significant zeros among all inputs. We also define the effective input cycles (EIC) as the minimum number of required cycles to feed effective bits of all inputs into a fragment, which is equal to the maximum effective bits of all inputs corresponding to that fragment. For example, as shown in Figure 7, the effective bits of input 1 is 6, however, the required EIC for the fragment is 7. Because the input 2 has the largest effective bits in the fragment, which is 7. The EIC in the coarse-grained designs that have large fragment size (e.g., 128) is generally higher than the fine-grained designs that have smaller fragment size (e.g., 4, 8 or 16). The reason is that the larger fragments have a higher probability to contain the inputs that have higher effective bits. Figure 8 (a) shows an example of the percentage of EIC (1 to 16) of fragments using 16-bit inputs and various fragment sizes (i.e., 4, 8, 16, 32, 64, 128) in one CONV layer. As the fragment size becomes larger, it increases the percentage of the fragments that require more EIC. Figure 8 (b) shows, under different fragment sizes, the average required EIC over all fragments for different layers. For fragment size of 4, the average required EIC of all layers to feed all effective bits into crossbar is 10.7, which saves 33% of the total 16 cycles. The required EIC for fragment size of 128 is 15, which only saves 6% cycles. These results show that while zero-skipping is applicable to coarse-grain crossbars as well, the benefits are drastically less.

To take this key advantage, we propose a zero skipping logic as shown in Figure 9. It dynamically controls the input cycles to skip the redundant cycles for feeding zeros, which do not contribute to output, but consume power, energy and increase latency. As a result, FORMS achieves higher performance than the coarse-grained designs.

---

**Fig. 6:** Test accuracy under different fragment sizes on CIFAR-100 dataset.

**Fig. 7:** Input Effective Bits and Required Fragment EIC.

**Fig. 8:** (a) Percentage of effective input cycles for different fragment sizes using 16-bit input data; (b) average effective input cycles for various fragment sizes.

**Fig. 9:** Zero-skipping Logic.

---

C. Overall Architecture

FORMS includes several architectural and circuit-level optimizations. We performed design space exploration to find the best size of crossbar arrays, ADCs, DACs, and eDRAM storage. The FORMS system is organized into the multiple nodes/tiles as shown in Figure 10. Each layer of the CNN is mapped into one or multiple tiles. Tiles are connected together in a mesh-based network while the data flow between different layers (tiles) in a pipelined manner. The chip controller orchestrates the flow of operation between different tiles. Each tile comprises multiple MAC units (MCU), eDRAMs, and digital units (DUs) that contain shift and add units, activation function, and output registers. Each MCU comprises eight 128 × 128 crossbar arrays, ADC units, and output registers. For fragment sizes of 16, 8, and 4, FORMS employs 5, 4, and 3-bit ADCs. Unless mentioned explicitly, we assume the fragment size 8 in our discussion. In ISAAC, the 8-bit ADCs contribute to 58% of tile power and 31% of tile area consumption. If with the same technology, we build a 4-bit ADC, it results in almost 4× times less area and power [59, 60]. By reducing the ADC resolution from 8-bit to 4-bit, the throughput will drop by a factor of 16× since each time only one fragment (i.e., 8 rows) is activated for computing dot-products using 4-bit ADCs; whereas in ISAAC, 128 rows are processed each time. In FORMS, we use 2-bit ReRAM cells. Through design space explorations, we find that 2-bit ReRAM cells delivers a better energy-efficiency than other number of bits per cell (e.g., 4-bit, 8-bit). ADC bits increase as we increase the ReRAM cell bits, thereby consuming more power and area. More importantly, using more bits per ReRAM cells requires more rigorous hardware fabrication, which also introduces imprecision in analog computing and is more prone to process imprecision.

---

**Fig. 10:** Node architecture in FORMS.
ESULTS

V. EVALUATION RESULTS

In this section, we first evaluate our proposed FORMS optimization framework in terms of model accuracy and ReRAM crossbar reduction achieved by combining crossbar-aware structured pruning, polarization, and quantization techniques. And we compare our results with several representative pruning works. Then, we analyze our FORMS accelerator architecture design in terms of area, power, throughput, and performance rate, and compare the results with the state-of-the-art accelerator designs. At the end of this section, we analyze the impact of variation from both the software and hardware perspective. All the results of FORMS are based on 16-bit inputs/activations and 8-bit weights, and 2-bit ReRAM cells are used. The detailed experimental setups for the software and hardware results are illustrated in Section V-A and Section V-B.

A. Comparing Model Compression Methods

We evaluate our method using several representative benchmark networks, including LeNet-5, ResNet-18/50, and VGG-16, and using MNIST, CIFAR-10/100, and ImageNet datasets. The crossbar reduction results are from our crossbar-aware structured pruned, polarized, and quantized models comparing to the original baseline model using a splitting mapping scheme [47]. All models are trained on an 8× NVIDIA Quadro RTX 6000 GPU server by PyTorch API.

MNIST & CIFAR-10. Table I shows, on MNIST dataset using LeNet5, FORMS achieves 185.44× crossbar reduction, where 23.18× reduction comes from crossbar-aware structured pruning, 4× reduction comes from quantization, and 2× reduction from polarization by eliminating half of the crossbars to represent positive/negative weights. When fragment size is
TABLE I: The experimental results of FORMS on multi-layer network on small to medium datasets.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>GroupScissor [62]</td>
<td>99.17%</td>
<td>23.18 ×</td>
<td>4 ×</td>
<td>-0.92%</td>
<td>185.44 ×</td>
</tr>
<tr>
<td>TinyButAcc [47]</td>
<td>93.70%</td>
<td>50.85 ×</td>
<td>4 ×</td>
<td>-0.35%</td>
<td>406.8 ×</td>
</tr>
</tbody>
</table>

TABLE II: The experimental results of FORMS on multi-layer network on medium to large datasets. Top-5 accuracy is used for ImageNet dataset.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>ResNet50 [63]</td>
<td>67.62%</td>
<td>1.73 ×</td>
<td>-</td>
<td>0.76%</td>
<td>1.73 ×</td>
</tr>
<tr>
<td>our ResNet50</td>
<td>76.37%</td>
<td>6.65 ×</td>
<td>8 ×</td>
<td>-0.03%</td>
<td>53.2 ×</td>
</tr>
<tr>
<td>TinyButAcc [47]</td>
<td>77.35%</td>
<td>9.46 ×</td>
<td>8 ×</td>
<td>-0.10%</td>
<td>73.44 ×</td>
</tr>
</tbody>
</table>

TABLE III: FORMS MCU hardware specification and comparison with ISAAC.

<table>
<thead>
<tr>
<th>Component Parameter</th>
<th>FORMS (Fragment size 8)</th>
<th>ISAAC [18]</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>2.1GHz</td>
<td>1.2GHz</td>
</tr>
<tr>
<td>DAC</td>
<td>8×128</td>
<td>8×128</td>
</tr>
<tr>
<td>Spec Power (mW)</td>
<td>1.000015</td>
<td>0.000004</td>
</tr>
</tbody>
</table>

4 or 8, there is no accuracy degradation (in fact, the accuracy is higher than the original model since the pruning may reduce the overfitting), where there is a minor accuracy loss for the fragment size of 16. FORMS achieves a much higher crossbar reduction ratio than GroupSissor [62]. On CIFAR-10 dataset, we compare our results with several reference works. TinyButAcc [47] is a state-of-the-art ReRAM-based pruning work using ADMM. By taking the crossbar size into account, we achieve a similar crossbar reduction ratio from the pruning part as TinyButAcc, with a lower pruning ratio. This helps FORMS avoid unnecessary accuracy drop. By combining the fragment polarization and quantization, our overall crossbar reduction ratio is 2× higher than TinyButAcc with similar accuracy.

CIFAR-100 & ImageNet. Compared to CIFAR-10 dataset, the classification task on CIFAR-100 and ImageNet dataset is more complicated. Especially for ImageNet, there are fewer redundant weights. Thus, it is common to have a much smaller pruning ratio on CIFAR-100 and Imagenet dataset. As shown in Table II, on CIFAR-100 dataset, without accuracy loss or with minor accuracy loss, we achieve 6.65×(53.2 ×), 9.18×(73.44 ×) and 8.15×(65.20 ×) weight pruning ratio (crossbar reduction) on ResNet-18, ResNet-50 and VGG-16, respectively.

On ImageNet, we compare our results with references on ResNet-18. Since model accuracy is more sensitive to pruning ratio on ImageNet dataset, to achieve a higher overall crossbar reduction ratio and maintain model accuracy, we use a less aggressive pruning strategy. Compared to TinyButAcc, we achieve higher overall crossbar reduction (13.36 × and 16 ×) with higher or similar accuracy when using fragment size of 4 or 8. In summary, compared to state-of-the-art works, FORMS achieves high crossbar reduction with no or little accuracy loss.

B. Area and Power

We develop an in-house simulator to model access latency, energy, and area of all buffers, on-chip interconnects and crossbar arrays as well as the performance of FORMS. The back-end of the tool utilizes CACTI 7.0 [68], NVSIM, and NVSIM-CAM [69, 70] to provide a unified platform that can support both volatile and non-volatile memories with multi-banking properties. It can also model process variations of the size and the threshold voltage of transistors. We conservatively choose a 10% process variation for evaluations. We use the VTEAM ReRAM model [71]. The zero skipping logic is modeled in Verilog HDL and synthesized using Synopsys Design Compiler at 45nm technology and scaled down to 32nm. We follow the methodology of ISAAC paper to model max-pooling, shift-and-add, ADC, DACs, and activation functions. The energy and area of the max-pool and shift-and-add are adapted from ISAAC [18] while for ReLU activation function circuits we use the information provided in PRIME [17].
TABLE IV: Comparison of FORMS hardware characteristics with ISAAC and DaDianNao

<table>
<thead>
<tr>
<th>Architecture</th>
<th>GOPs ( \times )</th>
<th>Area ( \times )</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISAAC</td>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>DaDianNao</td>
<td>1/16</td>
<td>1/16</td>
<td>1/16</td>
</tr>
<tr>
<td>PUMA</td>
<td>0.13</td>
<td>0.45</td>
<td>0.58</td>
</tr>
<tr>
<td>TPU</td>
<td>0.79</td>
<td>0.79</td>
<td>1.58</td>
</tr>
<tr>
<td>WAX</td>
<td>0.08</td>
<td>0.48</td>
<td>0.56</td>
</tr>
<tr>
<td>WAX [74]</td>
<td>0.77</td>
<td>0.84</td>
<td>1.61</td>
</tr>
<tr>
<td>Pruned/Quantized-ISAAC</td>
<td>0.33</td>
<td>2.3</td>
<td>2.63</td>
</tr>
<tr>
<td>Pruned/Quantized-PUMA</td>
<td>0.34</td>
<td>0.08-2.5</td>
<td>2.88</td>
</tr>
<tr>
<td>FORMS (full optimization, 8)</td>
<td>36.02</td>
<td>27.73</td>
<td>63.75</td>
</tr>
<tr>
<td>FORMS (full optimization, 16)</td>
<td>39.48</td>
<td>51.26</td>
<td>90.74</td>
</tr>
</tbody>
</table>

TABLE V: Comparison of the effective peak nominal throughput per area unit and power unit of different architectures normalized to ISAAC.

<table>
<thead>
<tr>
<th>Architecture</th>
<th>GOPs ( w )</th>
<th>Area ( w )</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISAAC</td>
<td>1</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>DaDianNao</td>
<td>1/16</td>
<td>1/16</td>
<td>1/16</td>
</tr>
<tr>
<td>PUMA</td>
<td>0.13</td>
<td>0.45</td>
<td>0.58</td>
</tr>
<tr>
<td>TPU</td>
<td>0.79</td>
<td>0.79</td>
<td>1.58</td>
</tr>
<tr>
<td>WAX</td>
<td>0.08</td>
<td>0.48</td>
<td>0.56</td>
</tr>
<tr>
<td>WAX [74]</td>
<td>0.77</td>
<td>0.84</td>
<td>1.61</td>
</tr>
<tr>
<td>Pruned/Quantized-ISAAC</td>
<td>0.33</td>
<td>2.3</td>
<td>2.63</td>
</tr>
<tr>
<td>Pruned/Quantized-PUMA</td>
<td>0.34</td>
<td>0.08-2.5</td>
<td>2.88</td>
</tr>
<tr>
<td>FORMS (full optimization, 8)</td>
<td>36.02</td>
<td>27.73</td>
<td>63.75</td>
</tr>
<tr>
<td>FORMS (full optimization, 16)</td>
<td>39.48</td>
<td>51.26</td>
<td>90.74</td>
</tr>
</tbody>
</table>

charge pump circuit [72] is used to provide higher voltage as ReRAM cells require a write voltage more than the supply Vdd. The off-chip links are the same HyperTransport serial link used by ISAAC [18] and DaDianNao [67]. Also, the power and area of 1-bit DAC (a simple inverter) are adopted from [60]. The ADC energy and area are taken from [59]. To get power and area of the same style ADC used in ISAAC, but with 4-bit resolution, we scale down the power and area of the memory, clock, and \( v_{\text{ref}} \) buffer linearly, and the capacitive DAC exponentially [60]. The same scaling has been used in other works like ISAAC. We utilize a 4-bit ADC with 2.1 GSPs [73]. We choose this methodology to model peripheral circuitry and make a fair comparison at 32 nm with state-of-the-art works. We also compare the results with the fully digital DaDianNao [67], after scaling from 28nm to 32nm.

To make a fair ISO-area comparison on throughput and frame processing rate with ISAAC, we build FORMS to have similar power and area to ISAAC. We compare the power and area of the proposed building blocks in Table III. Table IV shows the area and power of the main components of FORMS, ISAAC and DaDianNao (digital design) without incorporating the pruning, and quantization, while the fragment is set to 8. Specifically, FORMS needs sign indicator arrays, and a few interconnects, which connect ADCs to fragments. It is noteworthy to mention that polarization helps to accommodate more weights in the same crossbar than existing techniques. In addition, since FORMS performs more computations than ISAAC, it needs higher bandwidth (512-bit versus 256-bit in ISAAC) and larger eDRAM to store the results(128KB vs. 64KB in ISAAC). However, since an ADC in FORMS generates 16 levels compared with 256 levels generated in ISAAC (due to using small fragment sizes), the required sample&hold circuit is smaller and faster. Overall, the sample&hold circuit in FORMS is almost 2× smaller than ISAAC. In addition, Zero-skipping logic saves dynamic power consumption by feeding fewer input bits (useless 0s) to the crossbar. In summary, we build FORMS to have almost the same power and area as ISAAC. The difference is negligible (0.08% more power and 4.5% more area). Like ISAAC and PUMA, in return for consuming more area and power compared with DaDianNao, the throughput of FORMS is increased significantly.

C. Throughput

Table V compares the peak nominal area-, power-efficiency of FORMS that uses the fragment size of 8 and 16 with state-of-the-art DNN accelerators in terms of the number of operations performed per second per \( \text{mm}^2 \) and the number of operations performed per watt (i.e. \( \frac{\text{GOPs}}{\text{mm}^2} \) and \( \frac{\text{GOPs}}{w} \)). The results are normalized to the ISAAC in terms of \( \frac{\text{GOPs}}{\text{mm}^2} \) and \( \frac{\text{GOPs}}{w} \), respectively. As results demonstrate, by taking advantage of the proposed pruning and quantization methods, the throughput of the ISAAC and PUMA are increased considerably. This potential increase can be achieved if interconnects can provide enough bandwidth for the processing crossbars. By only considering the polarization, the effective peak throughput of FORMS with the fragment size of 8 is 4.15×(1.36× 6.75×(1.27×) over DaDianNao and TPU, respectively. By increasing the fragment size, the throughput is increased. For example, when we increase the fragment size to 16, the throughput of FORMS with the polarization only is increased by 42% (29%). FORMS can outperform existing architectures when we apply all of the proposed methods including pruning, quantization, polarization, and zero-skipping logic. In terms of \( \frac{\text{GOPs}}{\text{mm}^2} \), FORMS with the fragment size of 16, outperforms the original non-pruned ISAAC and Pruned/Quantized ISAAC by 39× and 1.5×, respectively. These results in terms of \( \frac{\text{GOPs}}{w} \) are 51× and 1.9×. Overall, the peak throughput of the FORMS is higher than the existing designs. Note that WAX and SIMBA trade-off throughput for power efficiency by reducing voltage and frequency. For instance, in SIMBA, the voltage is 0.48V and frequency is 0.52GHz, whereas, in WAX, the frequency is 0.2GHz while the voltage is not mentioned.

D. Frame Processing Rate

Reaching the higher throughput per area unit and \( \text{fps} \) per area unit is not the only goal of an acceleration design [75, 76]. For instance, the throughput per area efficiency of commercial TPU [21, 76] is only 41\% \( \frac{\text{GOPs}}{\text{mm}^2} \). Moreover, many DNN-based applications take advantage of a higher frame per second (fps) speed up or end to end throughput. For example, object detection [77], GoTurn [78], self-driving cars [79], virtual and augmented reality applications [80] tend to have higher fps processing rate rather than higher throughput per area or power efficiency. This makes the high fps another crucial property for DNN accelerators.

We compare the frame per second speed up of different architectures when we apply assorted proposed techniques.
Fig. 13: Speed up results in terms of frame per second on CIFAR-10 when various techniques proposed in FORMS are applied.

Fig. 14: Speed up results in terms of frame per second on CIFAR-100 and ImageNet when various techniques proposed in FORMS are applied.

Table VI: Accuracy degradation caused by device variation for ResNet18 on different dataset under lognormal distribution with 0 mean and 0.1 standard deviation.

<table>
<thead>
<tr>
<th>Dataset</th>
<th>Original Model</th>
<th>Polarization Only</th>
<th>Pruning Only</th>
<th>Full Optimization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cifar10</td>
<td>0.35%</td>
<td>0.37%</td>
<td>1.82%</td>
<td>1.80%</td>
</tr>
<tr>
<td>Cifar100</td>
<td>0.72%</td>
<td>0.68%</td>
<td>1.86%</td>
<td>1.89%</td>
</tr>
<tr>
<td>ImageNet</td>
<td>2.87%</td>
<td>2.86%</td>
<td>4.24%</td>
<td>4.21%</td>
</tr>
</tbody>
</table>

E. Variation Analysis

Variation is a challenge in building in-situ accelerators [81]. We evaluate the impact of device variation of ReRAM device caused by the imperfection in fabrication technology. We model the device variation as a log-normal distribution [82]. Table VI shows the accuracy degradation of ResNet18 (other networks have similar results) on different datasets, when introducing a device variation with 0 mean and 0.1 standard deviation. The accuracy degradation is based on the accuracy results shown in Table I and II, and it is the average value of 50 runs. The classification task on ImageNet is much harder than Cifar10/100. It is more sensitive to the hardware variation [83]. For instance, the original model (without adopting any compression) has around a 2.8% accuracy degradation. As shown in Table VI, our polarization, quantization, and zero-skipping techniques do not decrease the network robustness, while the pruning introduces a certain degradation of robustness (an extra 1.5% accuracy degradation). The reason is that when 50% of the weights are pruned (under 2× pruning rate), each remaining weight becomes more important and the network resistance to variation reduces. But it happens in all pruning works and is not a problem unique to FORMS. The accuracy degradation can be relieved by reducing the prune ratio. Such a tradeoff depends on the demands of real applications. It is worth noting that the prior techniques used to improve robustness [29, 84, 85] can be applied to FORMS.

VI. Conclusion

We propose FORMS, a fine-grained ReRAM-based DNN accelerator with algorithm/hardware co-design optimizations. A novel fragment polarization method is proposed to elegantly solve the natural challenge of representing positive/negative weights on ReRAM crossbars without doubling crossbar cost or introducing extra hardware cost for result compensation. Weight pruning and quantization technique are combined to explore a good balance between the overall hardware cost and performance. We design a fine-grained architecture that is more robust to non-idealities and noise and makes the ADC implementation less challenging compared to the coarse-grained architecture designs. Crucially, our novel zero-skipping logic significantly avoids unnecessary computations and reduce computation time. Putting all together, our FORMS optimization framework can speed up ISAAC up to 377.9×. When combining our optimization framework and architecture design, FORMS achieves 1.50× and 1.93× area and power efficiency improvements in terms of \( \frac{GOPS}{mm^2} \) and \( \frac{GOPS}{W} \) over an optimized ISAAC with almost the same power/area costs.

ACKNOWLEDGEMENT

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REFERENCES

pruning and differential crossbar mapping for reram-based edge ai,” in 2021 22nd International Symposium on Quality Electronic Design (ISQED), 2021, pp. 135–141.


[56] Y.-C. Chen, C. Chen, C. Chen, J. Yu, S. Wu, S. Lung, R. Liu, and C.-Y. Lu, “An access-transistor-free (0/t1r) non-volatile resistance random access memory (rram) using a novel threshold switching, self-rectifying chalco-


