Extreme Low Power Technology using Ternary Arithmetic Logic Circuits via Drastic Interconnect Length Reduction

Kiyung Kim[1, 2], Sunmean Kim[3], Yongsu Lee[1, 2], Daeyeon Kim[4], So-Young Kim[1, 2], Seokhyeong Kang[4], Byoung Hun Lee*[1, 2]
[1]Center for Emerging Electric Devices and Systems,
[2]School of Material Science and Engineering, Gwangju Institute of Science and Technology
123 Cheomdangwagi-ro, Buk-gu, Gwangju, 61005, Republic of Korea
[3]Department of Electrical Engineering, Ulsan National Institute of Science and Technology
50, UNIST-gil, Ulju-gun, Ulsan 44919, Republic of Korea
[4]Department of Electrical Engineering, Pohang University of Science and Technology
77, Cheongam-ro, Nam-gu, Pohang, Gyeongbuk 37673, Republic of Korea

E-mail: bhl@gist.ac.kr

***Abstract*— Ternary logic is more power-efficient than binary logic because of lower device count required to perform the same logic functions. Its benefits become more pronounced in highly scaled systems where most power consumption occurs at the interconnect portion. We examined the benefits of ternary logic including the impacts of interconnect length reduction using a realistic ternary device model. The standard cell layouts of ternary SUM, NCARRY, NANY, and PROD gates are designed using balanced ternary logic and multi-threshold graphene barrister (MTGB). The interconnect wire length of the 5-trit arithmetic logic unit is reduced by ~37 % and this reduction rate is maintained even in more complex circuits.**

Keywords—low power technology, ternary logic, interconnect length

I. Introduction

Continuous scaling of silicon technology makes state-of-art node manufacturing less cost-effective and the design complexity has been increased by high power consumption. Especially, the portion of power consumption in the interconnect is rapidly increasing, but the technical progress in the interconnect has been slowed down due to the intrinsic material limit (resistivity and permittivity, Fig. 1 (a)) [1].

Thus, the reduction of interconnect burden using three-dimensional integration is getting more attention. TSV and some of 2.5D integration technology have been commercialized. Also, the recent progress in monolithic 3D integration is opening a window for diverse hybrid architectures such as logic-memory hybrid or logic-sensor hybrid architecture. In this sense, the upper level logic layer can adopt a drastically low power approach with slightly lower performance while the bottom logic layer maintains the system performance. For this approach, multi-valued logic (MVL) technology can be very attractive because of its strong competitiveness in power reduction and simple design.

Hurst showed that ternary logic is the most cost-effective system among MVLs (Fig. 1 (b)) [2]. Based on this argument, various kinds of devices and circuit designs have been proposed for ternary logic circuits. Quantum dot gate FET (QDGFET) is one of the most typical ternary devices. By using the intermediate state shown in the current characteristic curve, it was possible to implement ternary logic with a relatively small number of devices. However, in the case of ALU, such benefits are diminished because adder and multiplier are designed using decoders. In other approaches, carbon nanotube FETs (CNTFETs) were used to configure ternary logic using binary devices. This method used the multi-threshold voltage modulated by the diameter of carbon nanotube. Using CNTFETs with six different threshold voltages, stable ternary ALUs has been demonstrated [3]. However, the circuits using individually placed multi-threshold voltage CNTFETs are not compatible with the wafer-scale process and the circuit area can be large compared to binary devices due to the large number of devices used to configure ALUs. As such, although some studies have theoretically shown the advantages of ternary systems, several limitations hinder it from being realistic and reliable.

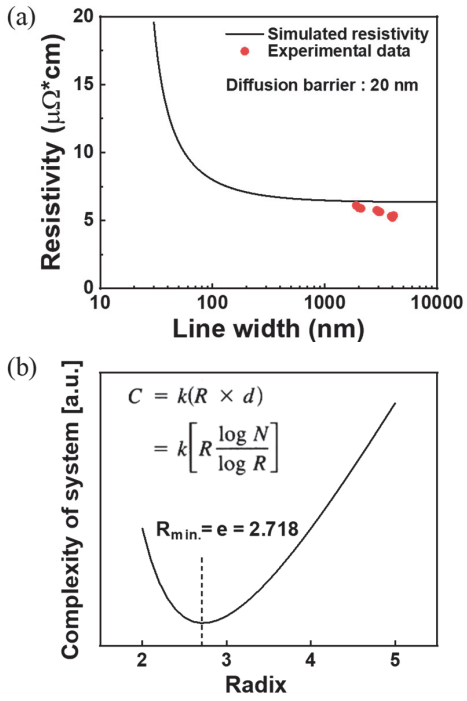

Figure 1. (a) Dramatic increase of interconnect resistivity at the nanoscale. (b) The complexity of system as an increase of system radix.

978-1-7281-5406-0/20/$31.00 ©2020 IEEE
DOI 10.1109/ISMVL49045.2020.00-13

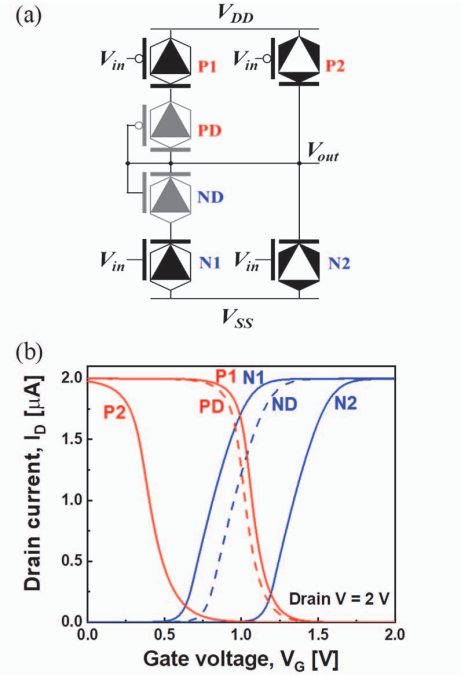

Figure 2. (a) The transistor level schematic of multi-threshold graphene barristor standard ternary inverter. In each hexagonal symbol, the colors mean threshold voltage. N, P mean the carrier type of graphene barristor. (b) Single device I_D-V_G curves of each graphene barristor in Fig. 2 (a). (Drain voltage=2 V)

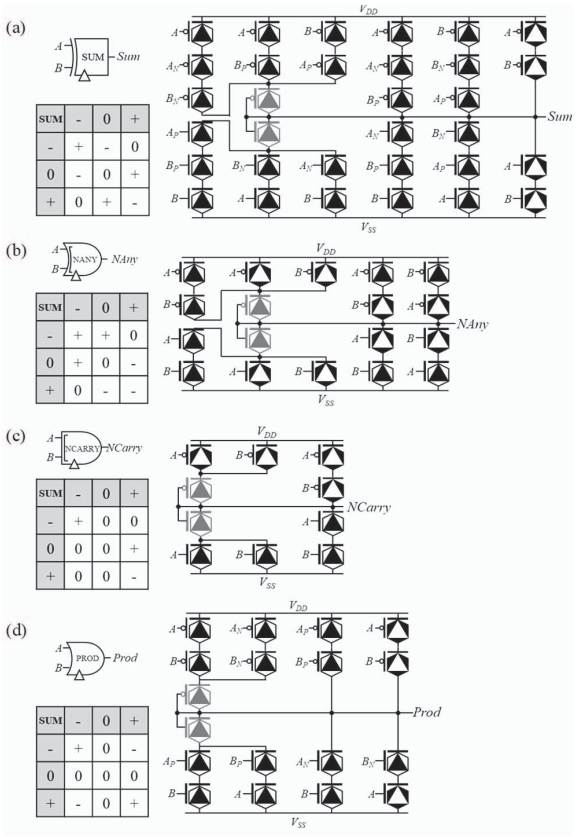

Figure 3. The gate symbol, truth table and transistor-level schematic of ternary (a) SUM gate, (b) NANY gate, (c) NCARRY gate, (d) PROD gate.

Recently, new multi-value logic devices aiming for more realistic implementation have been proposed, including ternary CMOS (TCMOS) and multi-threshold graphene barristor (MTGB) [4][5]. Also, in scaled device technologies, actual power consumption in back end of line (BEOL) interconnect is much greater than that in front end of line (FEOL) devices. Thus, the impacts of BEOL power consumption should be accounted when the benefits of ternary logic are considered in terms of device count reduction.

In this work, the realistic projection for interconnect wire lengths for the binary and ternary logic system has been investigated to assess the potential impacts on power consumption. Using the actual design rule of the binary system, the standard cell layouts of ternary SUM, NCARRY, NANY, and PROD gates are designed [6]. Then, the ternary adder/subtractor and multiplier are designed to assess the differences in the interconnect lengths. Based on these results, we compared the interconnect length of the 5-trit and 8-bit logic circuits. Finally, the interconnect wire lengths for the n-bit system have been investigated to assess the impacts on large scaled systems.

II. Standard Cell Layout Design

A. Ternary Arithmetic Logic Unit

To compare the interconnect length, we first designed the ternary arithmetic logic unit (ALU) gates that make up the full-adder and multiplier. The gates were designed using the multi-threshold graphene barristor (MTGB) models. Graphene barristor consists of Schottky junction between a graphene and semiconductor whose barrier height is electrically controlled by the gate bias [7]. Since the Schottky barrier height determines the drive current, very high on-off ratio can be obtained. The threshold voltage of this device can be controlled by setting the initial Fermi level of graphene using an extrinsic chemical doping process [8]. The ternary logic synthesis for MTGB is similar to that of CNTFET [9], but the fabrication process is more reproducible and wafer scale integration been demonstrated [5][8]. We adopted a balanced ternary approach because the balanced ternary(use +, 0, -) has a symmetrical pull-up and pull-down area, which is advantageous for layout design and allows the fabrication of multipliers with fewer devices compared to unbalanced ternary (use 0, 1, 2) [9][10].

Fig. 2 shows the general operating principle of MTGB ternary logic. The standard ternary inverter is shown in Fig. 2 (a), and the symbol with the triangle in hexagon means a graphene barristor. The colors of triangle represent the different threshold voltage of barristor: black, gray, and white mean $|V_{DD} - V_{th,0}|$, $|V_{DD}/2|$, $|V_{th,0}|$, respectively. They are also named as N1, N2, ND, P1, P2 and PD depending on the carrier type and threshold voltage. As shown in Fig. 2 (b), N1 and P1 make the intermediate state when the input voltage is half V_{DD}. ND and PD receive negative feedback to keep the middle state stable at half V_{DD}. N2 and P2 load output node into V_{DD} and V_{SS} at pull-up and pull-down states.

Four more ternary logic gates are necessary to make the ternary adder/subtractor and multiplier. Fig. 3 shows the truth table and circuit diagram of them. Subsequent ALU gates were also designed in this way using six different threshold

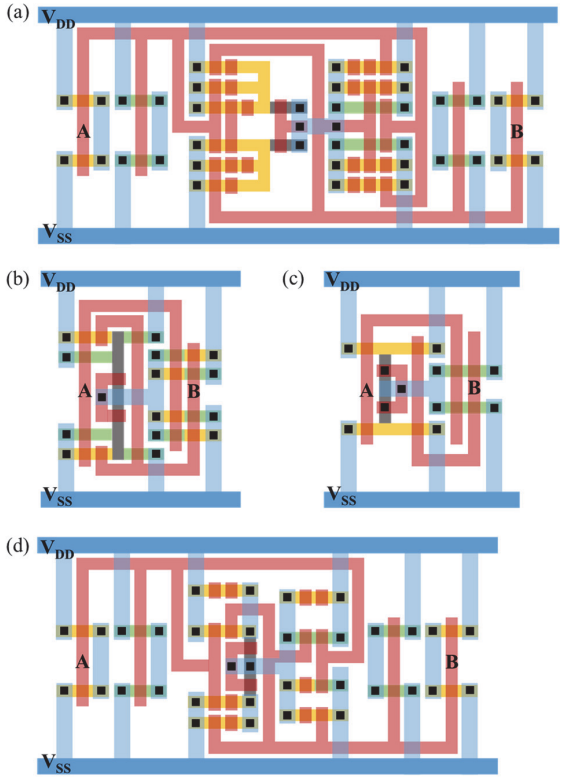

Figure 4. The Standard cell layout of (a) SUM gate, (b) NANY gate, (c) NCARRY gate, (d) PROD gate. Designed under CMOS layout design rules, assuming a minimum feature size λ. (Blue line: M1, red line: poly-Si gate, yellow, gray, and green line: $|V_{DD} - V_{th,0}|$, $|V_{DD}/2|$, $|V_{th,0}|$ graphene barristor.

voltages of graphene barristor. The operation and power-delay product (PDP) of these logic gates were demonstrated by PSPICE simulation [5].

B. Standard Cell Layout

A standard ternary cell layout is designed to determine the length/width ratio of layouts and the locations of metal line contacts. The standard cell layouts of the SUM, NANY, NCARRY, PROD gates are shown in Fig. 4. Although the layout was designed for the graphene barristor process, the basic design rule of CMOS layout was considered in align margin, line width, and arrangement. The blue line means a metal 1(M1) line, and the red line means a poly-Si gate. The yellow, gray, and green line means $|V_{DD} - V_{th,0}|$, $|V_{DD}/2|$, $|V_{th,0}|$ graphene barristor line, respectively. Two negative ternary inverter(NTI)s and two positive ternary inverters(PTI)s were placed on both sides of SUM and PROD gates, since the input through NTI(A_N, B_N) and PTI(A_P, B_P) are needed. The input signal A and B were transferred to the polysilicon line, but the A_N, B_N, A_P, and B_P were connected to each transistor using M2 and M3 line.

III. Interconnect Comparison

A. 5-trit ALU System Design

The Interconnect length was compared between binary 8-bit and ternary 5-trit ALU system. Since 2^8 is 256 and 3^5 is 243, it can be assumed that both systems process similar amounts of information. Therefore, we designed a 5-trit

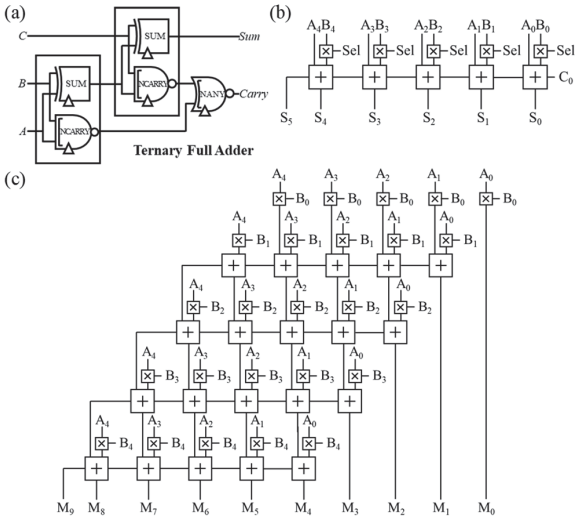

Figure 5. (a) The gate-level schematic of ternary full adder. (b) The schematic of 5-trit ternary adder/subtractor. (c) The schematic of the 5-trit ternary multiplier. (Large cross box: ternary full adder, small X box: PROD gates)

TABLE I. Comparison of Binary and Ternary Interconnect Wire Length

(Unit : μm)		M2	M3	Total
Adder/ Subtractor	8-bit	150	174	324
	5-trit	239	89	328
Multiplier	8-bit	1194	1196	2389
	5-trit	1047	457	1504

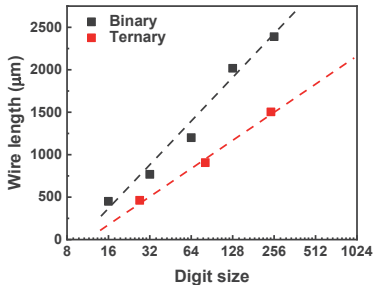

Figure 6. Total wire length estimation in the binary and ternary multiplier. The labels on the X-axis is a decimal number.

ternary adder and array multiplier [11], and the result is shown in fig. 5. In fig. 5 (b) and (c), the large cross box means the ternary full adder (Fig. 5 (a)), and the small box with the X symbol is the PROD gate. M2 and M3 lines were used to connect each cell and these lines are the largest part of the total interconnect length.

B. Calculation of Total Interconnect Length

For the realistic comparison with the binary system, the ternary interconnect wire length was estimated using the 65nm TSMC open library process design kit. The interconnect wire length of binary logic circuits was extracted using Cadence Innovus auto-placement & routing. Since the 65nm node

integration process for a graphene barristor is not feasible yet, we modified the ternary device model developed from the experimental data obtained from long channel graphene barristors. Nevertheless, this approach is still meaningful because 65nm node CNTFET model can be used in similar way [9][12].

There is no auto place & route tool that supports the physical design of ternary logic circuits. Therefore, we designed a custom layout based on the coordinates of the metal 1 polygon of each ternary standard cell to estimate the wire length of the ternary adders and multipliers. Based on the 1-trit designs, the placement and routing of the 5-trit ALU system (5-trit adder and 5-trit multiplier) was performed as shown in the gate-level schematic in Fig. 5.

Table I reports the result of the comparison between 8-bit binary and 5-trit ternary. In the case of the adder, the difference is not significant and the ternary interconnect is longer. However, in the multiplier, there is a big difference in the length of M3 line, which results in a total wire length reduction of 37 % compared to that of binary circuit. This is because the adders are arranged one-dimensionally, but the multipliers are connected in the two-dimensional array. In other words, the gain of the ternary circuit is greater under conditions that require more complex arrangements and connections. This result is very encouraging because most of area, power, and speed in an ALU are determined by the multiplier.

We have projected this model for higher digit size conditions using several data points for 4 - 8 bits (16 – 256) equivalent systems as shown in Fig. 6. As the digit size increases, the interconnect wire length increases with a logarithmic function. In spite of the increase in digit size, a certain percentage reduction of interconnect wire length is maintained in a high complexity system, confirming that the benefits of ternary logic technology will be maintained even after including the contribution of BEOL power consumption.

IV. Conclusion

Using the interconnect model for 65nm CMOS technology and realistic ternary device models, we have shown that ternary logic can reduce the interconnect length by 37% compared to that of binary logic at 5-trit or higher ALU level complexity. This result confirms that ternary logic architecture has a very strong advantage over binary logic architecture for extremely low power technology.

Acknowledgment

This research was supported by Nano-Material Technology Development program (2016M3A7B4909942), and Creative Materials Discovery Program (2017M3D1A1040828) through the National Research Foundation of Korea (NRF) funded by the Ministry of Science and ICT, Korea.

References

[1] M. T. Bohr, “Interconnect scaling-the real limiter to high performance ULSI,” in Proceedings of International Electron Devices Meeting, pp. 241–244, 1995.

[2] S. L. Hurst, “Multiple-Valued Logic—its Status and its Future,” IEEE Transactions on Computers, vol. C–33, no. 12, pp. 1160–1179, Dec. 1984.

[3] M. Moaiyeri, R. Mirzaee, K. Navi and O. Hashemipour, "Efficient CNTFET-based Ternary Full Adder Cells for Nanoelectronics", Nano-Micro Letters, vol. 3, no. 1, pp. 43-50, 2011.

[4] J. W. Jeong et al., “Tunnelling-based ternary metal–oxide–semiconductor technology,” Nature Electronics, vol. 2, no. 7, pp. 307–312, Jul. 2019

[5] S. Heo et al., “Ternary Full Adder Using Multi-Threshold Voltage Graphene Barristors,” IEEE Electron Device Letters, vol. 39, no. 12, pp. 1948–1951, Dec. 2018.

[6] N. Weste and D. Harris, CMOS VLSI design, 4th ed. 2009.

[7] H. Yang et al., “Graphene Barristor, a Triode Device with a Gate-Controlled Schottky Barrier,” Science, vol. 336, no. 6085, pp. 1140–1143, Jun. 2012.

[8] S. Kim et al., "Threshold Voltage Modulation of a Graphene–ZnO Barristor Using a Polymer Doping Process", Advanced Electronic Materials, vol. 5, no. 7, p. 1800805, 2019.

[9] S. Kim, T. Lim, and S. Kang, “An optimal gate design for the synthesis of ternary logic circuits,” in 2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC), 2018, pp. 476–481.

[10] H. Gundersen and Y. Berg, “A Balanced Ternary Multiplication Circuit Using Recharged Semi-Floating Gate Devices,” in 2006 NORCHIP, pp. 205–208, 2006.

[11] Guoping Wang and J. Shield, “The efficient implementation of an array multiplier,” in 2005 IEEE International Conference on Electro Information Technology, pp. 5, 2005.

[12] A. D. Franklin et al., “Sub-10 nm Carbon Nanotube Transistor,” Nano Lett., vol. 12, no. 2, pp. 758–762, Feb. 2012.

[13] C. Soldano, S. Talapatra and S. Kar, "Carbon Nanotubes and Graphene Nanoribbons: Potentials for Nanoscale Electrical Interconnects", Electronics, vol. 2, no. 4, pp. 280-314, 2013.

[14] S. Lin, Y.-B. Kim, and F. Lombardi, “CNTFET-Based Design of Ternary Logic Gates and Arithmetic Circuits,” IEEE Transactions on Nanotechnology, vol. 10, no. 2, pp. 217–225, Mar. 2011.