

# PIMnast: Balanced Data Placement for GEMV Acceleration with Processing-In-Memory

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**Abstract**—With unprecedented demand for generative AI (GenAI) inference, acceleration of primitives that dominate GenAI such as general matrix-vector multiplication (GEMV) is receiving considerable attention. A challenge with GEMVs is the high memory bandwidth this primitive demands. Multiple memory vendors have proposed commercially viable processing-in-memory (PIM) prototypes that attain bandwidth boost over processor via augmenting memory banks with compute capabilities and broadcasting same command to all banks. While proposed PIM designs stand to accelerate GEMV, we observe in this work that a key impediment to truly harness PIM acceleration is deducing optimal data-placement to place the matrix in memory banks. To this end, we tease out several factors that impact data-placement and propose PIMnast methodology which, like a gymnast, balances these factors to identify data-placements that deliver GEMV acceleration. Across a spectrum of GenAI models, our proposed PIMnast methodology along with additional orchestration knobs we identify delivers up to  $6.86\times$  speedup for GEMVs (of the available  $7\times$  roofline speedup) leading to up to  $5\times$  speedup for per-token latencies.

**Index Terms**—Generative AI, GEMV, Processing-in-Memory

## I. INTRODUCTION

Generative AI (GenAI), powered by transformer architecture, has revolutionized human-computer interactions with its ability to respond to natural language prompts. However, unlocking the promise of GenAI will necessitate that a non-trivial subset of above AI capabilities be executed locally on edge/client devices (e.g., laptops, automotive compute, etc.). Motivations for this are manifold: steep costs (e.g., a traditional search query costs 10x less and consumes 100x lower energy as compared to one powered by cloud GenAI) [1]–[3], better personalization via access to rich user context, stronger privacy preservation, and lower latency. As such, in this work, we focus on the deployment of such GenAI techniques on client devices, specifically, laptops.

An important primitive that dominates GenAI inference is general matrix-vector multiplication (GEMV) and a key characteristic this primitive manifests is the high memory bandwidth it demands. A promising technology which stands to deliver acceleration for GEMV primitives via memory bandwidth boost is processing-in-memory (PIM). Multiple memory vendors have proposed commercially viable PIM prototypes that, via augmenting memory banks with compute capabilities and broadcasting same command to all banks, attain bandwidth boost over processor that only accesses a memory bank at a

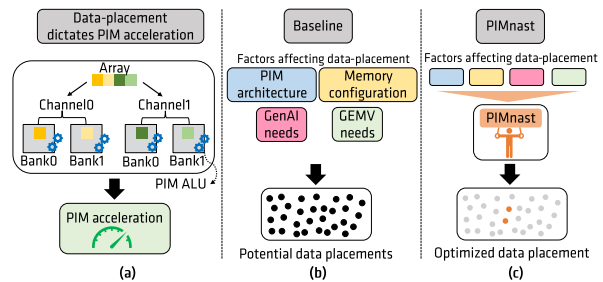


Fig. 1: PIMnast balances myriad factors to identify data-placement delivering GEMV-PIM acceleration.

time. While proposed PIM designs<sup>1</sup> stand to accelerate GEMV, we observe in this work that a key impediment for attaining PIM acceleration is deducing optimized data-placement to place the matrix in memory banks.

Traditional processors such as CPUs and accelerators such as GPUs decouple computation units (e.g., cores, compute units in GPUs) and memory allowing any computation unit to access any memory module (e.g., channels/banks). In contrast, as depicted in Figure 1a, PIM closely couples computation unit (PIM ALU) and associated memory (e.g., memory bank in commercial PIM prototypes) with the computation unit only accessing data present in associated memory module. By localizing the ALUs and data, along with broadcasting same command to all memory modules, PIM attains memory bandwidth boost over processor. However, this collocation requires further thought to what data is placed in which module.

Given the importance of data-placement in determining resultant PIM acceleration, in this work we first tease out myriad factors that impact data-placement. We identify four key categories of factors depicted in Figure 1b which lead to a rich space of potential data-placements. Specifically, PIM architecture (e.g., PIM ALU design, load-balancing over memory banks, etc.), memory configuration (e.g., data interleaving, row buffer locality, etc.), application/ML needs (e.g., data-formats, scale-factors, etc.), and GEMV needs (e.g., shape/size of GEMV). We discuss how each of these factors places

<sup>1</sup>Note, we consciously choose to confine our work to memory vendor proposed, and hence commercially viable, PIM prototypes and focus on maximizing GEMV acceleration for these prototypes.

unique demands on an optimized data-placement.

Armed with above holistic view of factors of import, we propose **PIMnast** methodology (Figure 1c), which like a gymnast, balances said factors and their demands to help identify data-placement that delivers PIM acceleration. We present algorithms which help guide the choice of data-placement and discuss system implications of attaining said data-placement. Additionally, we also identify orchestration knobs which deliver further PIM acceleration via careful scheduling of computation and resource management to facilitate reuse.

Overall, key contributions of this work are:

- This work focuses on maximizing acceleration for GEMV, a critical GenAI primitive, using commercial processing-in-memory (PIM) solutions. To this end, we argue that data-placement has a major impact on resultant PIM acceleration and as such, we carefully tease out factors which affect data-placement and identify their intricate interplay.
- Armed with above holistic view, we propose **PIMnast**, a methodology which, like a gymnast, balances above myriad factors to guide data-placements which maximizes GEMV-PIM acceleration under given set of architecture and application constraints.
- We also identify that optimized data-placement can be coupled with meticulous computation orchestration and resource management to deliver further PIM acceleration via exploiting reuse.
- Our analysis with GEMVs manifesting in variety of GenAI models demonstrates that our proposed PIMnast methodology coupled with orchestration knobs we identify attains up to  $6.86\times$  speedup for GEMVs of the available  $7\times$  roofline speedup leading to up to  $5\times$  end-to-end speedup for per-token latencies.

## II. BACKGROUND

### A. GEMV: Memory Bandwidth-bound GenAI Primitive

Transformer architecture powered GenAI inference, depicted in Figure 2a, comprises both compute-heavy prompt phase (process user specified natural language prompt) and memory-bandwidth-heavy token generation phase (generate response to user prompt a token at a time). Token generation dominates the runtime (Section VI) specifically for client/edge scenarios (e.g., laptops, the focus of this work) where opportunities for batching multiple user requests are low. Especially with batch-size 1 (typical for laptop scenarios), token generation is dominated by general matrix-vector (GEMV) computations. As GenAI models of interest are comprised of billions of parameters, they manifest large memory footprints (typically several GB or more), rendering caches ineffective and resulting in DRAM bandwidth becoming a limiting factor. As an example, the token generation phase of a single 13B parameter model alone can consume as much as 120 GB/s of DRAM bandwidth considering 100ms per generated token, even with optimistic assumptions about software optimizations

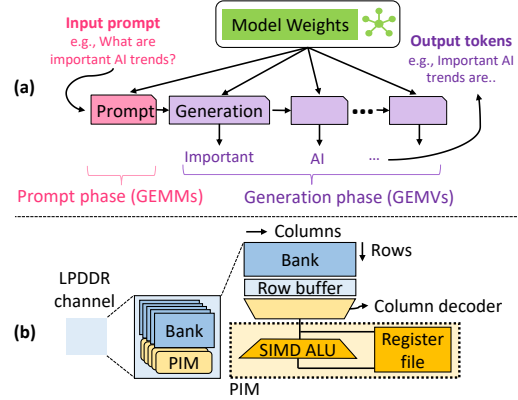


Fig. 2: (a) GenAI inference phases. (b) LPDDR-PIM overview.

to reduce auxiliary data structures associated with the model. In other words, a single GenAI model could consume the entire DRAM bandwidth of all but the highest end laptops, to say nothing of supporting other user applications (gaming, video playback, etc.), display, and other activity in the system concurrently. As GenAI continues to proliferate, accelerating memory bandwidth-bound GEMVs that dominate inference is critical to truly democratize GenAI productivity gains.

### B. Commercial PIM Prototypes

Recently, multiple memory vendors like Samsung and SK Hynix have proposed commercially viable processing-in-memory (PIM) designs that can be integrated with HBM [4] as well as LPDDR [5] and GDDR [6] memory. These designs place a computation unit/ALU near memory banks as we depict in Figure 2b for LPDDR memory.

Baseline LPDDR memories are comprised of independent channels and multiple banks therein. A read (or write) access, causes a specific DRAM row in a specific bank to be *activated*, wherein a data in the row is read out to *row-buffer* associated with the bank. Subsequently, a column access command reads a specific DRAM word (typically 256bits) from the row-buffer over the shared data-bus in the channel. In contrast, with PIM, higher effective bandwidth can be attained by activating same row across all banks (*all-bank row activation*) followed by broadcasting same column command in parallel to all banks. This leads to memory bandwidth boost commensurate to number of banks (typically 16 banks per channel) and PIM command rate (typically 2x lower than baseline reads/writes [4]), about 4-8x in practice as demonstrated by PIM prototypes.

The computation unit near memory banks comprise a SIMD ALU and register file. Further, as only parts of applications which demand high memory bandwidth are offloaded to PIM, interoperability with SoC (CPUs, GPUs, etc.) is paramount. Consequently, PIM designs lack sophisticated instruction orchestration capabilities and instead are controlled via read/write like fine-grain PIM commands from the processor. Finally, data consistency between processor and PIM is typically enforced in software (e.g., cache flushes).

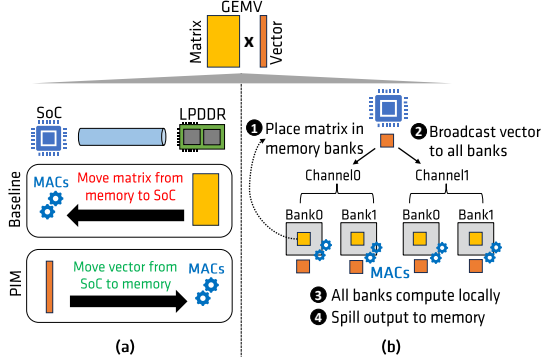


Fig. 3: (a) Baseline vs. PIM GEMV. (b) Steps in PIM GEMV.

### III. GEMV-PIM PERFORMANCE DETERMINANTS

#### A. Mapping GEMV to PIM

As discussed in Section II, large GEMVs that manifest in GenAI demand high memory bandwidth and can benefit via offload to PIM. We depict in Figure 3a an illustration of GEMV in baseline versus PIM. GenAI inference workflow for token generation (Section II-A) comprises sequence of GEMVs (weight matrix  $\times$  input vector) with interspersed vector operations (e.g., layer normalization, softmax, etc.). In steady state for baseline system, the key performance determinant is reading of large weight matrices from memory into the SoC as depicted. In contrast, with PIM, the weight matrices are left stationary in memory, while the SoC broadcasts vector elements in parallel to memory banks which then compute on them in parallel.

We also depict the four key steps in GEMV orchestration with PIM (GEMV-PIM) which are common for available commercial PIM prototypes in Figure 3b. First, weight matrices are appropriately placed in memory banks ❶, which we term as *data-placement*. Second, the SoC (CPU/GPU etc.) broadcasts vector elements to banks in parallel ❷ which are stored in near-bank structures (e.g., registers). This is followed by broadcasting MAC (multiply-accumulate) commands to banks in parallel ❸ causing each bank to multiply weight element in memory to vector element in register. Finally, after multiple MAC operations, an output element is ready, which is then spilled to memory ❹.

#### B. GEMV-PIM Performance Determinants

GEMV-PIM acceleration is determined by harnessing PIM memory bandwidth boost to the fullest while overcoming any potential overheads. Specifically, **data-placements** which (a) allow command broadcasts across all banks, and (b) avoid any data-movement between banks or between memory/SoC are best suited to harness PIM memory bandwidth boost. Additionally, every DRAM row activation in memory incurs row-open overheads. Consequently, data-placements which allow processing an open DRAM row in its entirety in every bank before opening another row will incur less row-open

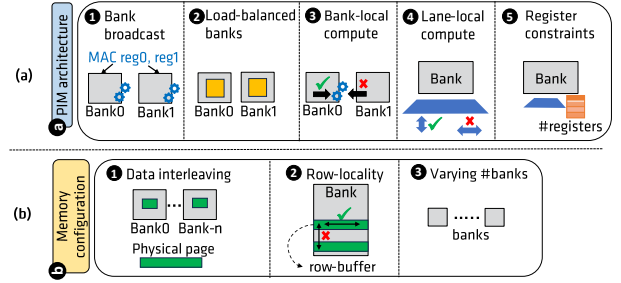


Fig. 4: Factors impacting data-placement.

overheads which eat into PIM acceleration. As such, optimized data-placements are critical to attaining PIM acceleration.

Unlike traditional architectures, where **computation orchestration** or scheduling of compute commands is not as dependent on data-placement in memory (e.g., sort using quick-sort or heap sort), in PIM, computation orchestration often follows from how data is placed in memory. This is so as orchestration is constrained to command broadcasts over banks to harness memory bandwidth boost. Nevertheless, within this limited space, tuning computation orchestration to better exploit reuse can lead to better performance. As an example, an orchestration mechanism which reuses broadcasted vector elements (Figure 3b) can lead to better PIM performance.

#### C. Factors affecting Data-placement

Next, we carefully tease out factors that need to be balanced for optimized data-placement for GEMV-PIM acceleration. We group them into four categories and identify interdependencies amongst them.

1) *PIM Architecture*: We depict ways in which PIM architecture dictates optimized data-placement in Figure 4a. As discussed, memory bandwidth boost is the key PIM benefit and as such data-placements which allow same command to be broadcasted to memory banks ❶ lead to better performance. Further, as memory banks are compute workhorses in PIM, data-placements which load-balance GEMV computation ❷ are also preferred for better performance. Current commercial PIM prototypes do not provision high-speed bank-to-bank communication and as such data-placements which avoid cross-bank communication are preferred ❸. Notice that load-balanced banks and avoiding cross-bank communication can conflict with each other. Of the two commercial PIM prototypes, Samsung design does not provision for cross-SIMD-lane communication requiring costly shift operations (e.g., to reduce data in multiple lanes). As such, data-placements which avoid cross-SIMD-lane communication also lead to better performance in this design ❹. Finally, PIM designs provision for limited scratchpad space (e.g., registers) near PIM ALUs. As such, data-placements which work within these constraints are the only ones that can be exercised ❺.

2) *Memory Configuration*: We depict ways in which memory configuration dictates optimized data-placement in Figure 4b. First, physical pages are often interleaved across banks in the system ❶ to maximize channel/bank parallelism

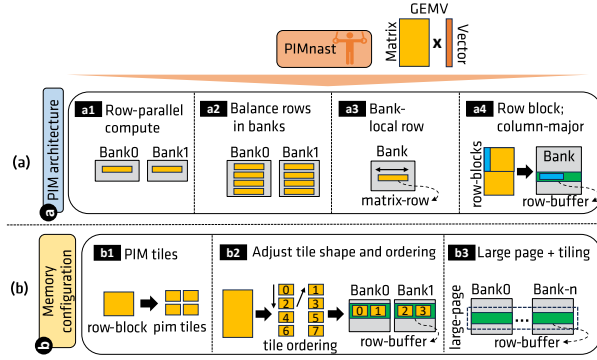


Fig. 5: Tackling of data-placement factors with PIMnast.

and data-placements have to be cognizant of this. Second, every time a DRAM row is activated, row-open overheads are incurred. As such, data-placements which fully process an open row before opening another ②, thus incurring low row-opens overall, lead to better performance. Finally, systems provision for different number of channels, and hence banks, which an optimized data-placement has to be cognizant of ④.

3) *GenAI Needs*: Model scaling is one of the key factors contributing to disruptive capabilities of GenAI models. As memory capacity fails to keep up with this scaling [7], innovations in data-formats (e.g., BF16, INT8, INT4) have been relied on. Low precision data-formats lower memory capacity needs allowing larger models to be deployed even on client devices. Additionally, they can also harness higher compute throughput that low-precision format avails. Data-placement has to be cognizant of data-format under consideration. Further, low-precision inference often relies on block-level scale-factors [8] and metadata which also has to be appropriately placed in memory. In the context of GEMV, with block-level scale-factors, computation of single output element is interspersed with multiplication of partial outputs with both weight and input-vector scale-factors.

4) *GEMV Needs*: Finally, GEMVs manifested in realistic applications come in all shapes/sizes and this has to be factored in data-placement. While factoring GEMV shapes/sizes is also challenging in baseline designs, above highlighted factors further complicate this in context of PIM.

#### D. Factors affecting Orchestration

As discussed in Section III-B, in PIM, computation orchestration follows from data-placement chosen and is constrained by the command broadcast requirement in PIM. That said, exploiting reuse (e.g., input vector reuse) for better PIM acceleration can lead to alternate orchestrations. Similarly, local scratchpad (e.g., registers) allocation to temporary data can also affect resultant PIM performance and lead to alternate orchestrations.

### IV. PIMNAST: GEMV-PIM DATA-PLACEMENT

We discuss in this section our methodology **PIMnast**, which balances the myriad factors we discussed in Section III-C

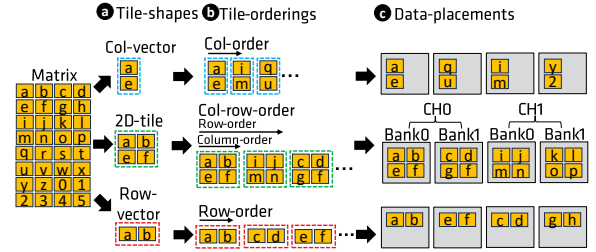


Fig. 6: Decoupling tile-shape and tile-order leads to nine possible data-placements (three are depicted).

to help guide an optimized data-placement for GEMV-PIM. We focus in this section on deducing the optimized data-placement and defer software considerations to realize said data-placement to Section V-A. Further, we first begin via intuitively discussing data-placement choices we make which directly address the factors we identified in Section III-C. We follow this with *matrix tiling and tile-ordering* which provides a framework to realize our data-placement choices.

#### A. Tackling GEMV-PIM Data-placement Factors

1) *PIM Architecture*: We depict our data-placement choices to tackle PIM architecture factors in Figure 5a. We number each choice to match the factor it addresses in Figure 4. Since each matrix row in GEMV matrix independently interacts with input vector, to maximize bank broadcasts, we distribute matrix rows over banks ①. As such, post broadcasting input vector to banks, each bank can independently work on separate matrix rows but harness command broadcasts. To load-balance GEMV-PIM, we attempt to equalize matrix rows amongst banks ②. To avoid cross-bank communication we attempt to ensure a single matrix row is mapped to single bank in entirety ③<sup>2</sup>. Finally, to overcome the overheads associated with cross-SIMD-lane computation, we block rows in a matrix and distribute resultant *row-blocks* amongst banks when possible. This allows us to have a column-major layout within row-block ④ such that SIMD lanes are each working on different output elements avoiding cross-SIMD lane communication. Finally, we incorporate register constraints in our data-placement algorithms to honor them (Section IV-B).

2) *Memory Configuration*: We tackle interleaving of data across banks via tiling the matrix (Figure 5b ⑤) and picking the tile-size to match data interleaving granularity (e.g., 256 bytes) of the underlying memory system.

Harnessing DRAM row-locality requires that tiles belonging to same matrix row-block be placed consecutively in a row-buffer within a bank. To do so, we first observe that in presence of tiling, traditional matrix data-placement formats such as row-major and column-major, couple *tile-shape* and *tile-order*. That is, column-major placement can be considered to be column-vector tiles (tile-shape) coupled with column-order (tile-order) placement (Figure 6 top). Similarly, row-major placement can be considered to be row-vector tiles

<sup>2</sup>Note, certain GEMV shapes/sizes make this challenging. We discuss these scenarios in Section VI-F.

(tile-shape) coupled with row-order (tile-order) placement of tiles (Figure 6 bottom). By decoupling tile-shape from tile-order, with multiple tile-shapes (column-vector, row-vector, 2D-tile) and multiple tile-orders (column-order, row-order, column-row-order), we can better control tile placement to attain DRAM row-locality [b2](#). Overall, *by decoupling tile-shape and tile-order*, we can unlock a rich space of data-placement possibilities (nine in all, three depicted in Figure 6) and we discuss algorithms in Section IV-B which help walk this space judiciously and help us attain DRAM row-locality.

To tackle varying banks in the system, we incorporate number of banks in our tile-order algorithm (Section IV-B2). Additionally, to better control DRAM row-locality in presence of varying banks we propose to employ large pages in the context of PIM [b3](#). We discuss page-size necessary to cover range of memory configurations in Section V-A.

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#### Algorithm 1 Find tile-shape

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1: Define:
2: W -  $M \times K$  weight matrix, IV -  $K \times 1$  input vector, OV -  $M \times 1$ 
   output vector
3: in_dform -  $W/IV$  data-format, out_dform -  $OV$  data-format (bit)
4: inter_gran - memory interleaving granularity (bit), tot_bank -
   total number of banks
5: tot_reg - total number of PIM registers, reg_size - size of each
   register (bit)
6: Tile -  $m\_tile \times k\_tile$ 
7: function GETPARAM
8:   Input:  $M, K, in\_dform, out\_dform, inter\_gran, reg\_size,$ 
    $m\_tile, k\_tile$ 
9:   Output:  $in\_reg, out\_reg$ 
10:   $in\_reg\_tot = (k\_tile \times in\_dform) / reg\_size$ 
11:  // Allow reuse of input reg space
12:   $in\_reg = \lceil (in\_reg\_tot \times reg\_size) / inter\_gran \rceil$ 
13:   $out\_reg = \lceil (m\_tile \times out\_dform) / reg\_size \rceil$ 
14:  return ( $in\_reg, out\_reg$ )
15: function GETTILESHAPE
16:   Input:  $M, K, in\_dform, out\_dform, inter\_gran, reg\_size,$ 
    $tot\_bank, tot\_reg$ 
17:   Output:  $m\_tile, k\_tile$ 
18:    $elem\_per\_tile = inter\_gran / in\_dform$ 
19:    $m\_tile = elem\_per\_tile$ 
20:    $k\_tile = elem\_per\_tile / m\_tile$ 
21:   while  $m\_tile \geq 1$  do
22:     // Test even-distribution
23:     if  $M \% (tot\_bank \times m\_tile) == 0$  then
24:        $in\_reg, out\_reg = getParam()$ 
25:       // Test reg availability
26:       if  $(in\_reg + out\_reg) \leq tot\_reg$  then
27:         // Tile-shape passing both tests
28:         return ( $m\_tile, k\_tile$ )
29:       else if  $m\_tile > 1$  then
30:          $m\_tile = m\_tile / 2$ 
31:          $k\_tile = elem\_per\_tile / m\_tile$ 
32:       else
33:         return ( $m\_tile, k\_tile$ )
34:       else if  $m\_tile == 1$  then
35:         return ( $m\_tile, k\_tile$ )
36:       else
37:          $m\_tile = m\_tile / 2$ 
38:          $k\_tile = elem\_per\_tile / m\_tile$ 

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3) *GenAI Needs:* To tackle data-format needs of GenAI, we parameterize our matrix tiling and ordering algorithms to factor data-format under consideration. Finally, to tackle metadata associated with weight matrices (e.g., scale-factors for low-precision formats), we interleave weights and associated scale-factors at memory interleaving granularity chunks to preserve DRAM row-locality. That is, via fine-grain interleaving we maximize the probability that weights and their associated metadata map to the same DRAM row thus attaining row-locality for PIM computation.

4) *GEMV Needs:* To tackle GEMV shapes/sizes we similarly parameterize our matrix tiling and ordering algorithms to factor matrix dimensions.

#### B. Matrix Tiling and Ordering

We discuss algorithms to pick tile-shape and tile-order that balances data-placement factors we identified above. Note that, to work with and not affect the interleaving granularity of underlying memory system, we set the tile-size to match interleaving granularity size.

1) *Tile-shape Algorithm:* Algorithm 1 depicts our tile-shape picking methodology. Recall that, we aim to distribute and balance matrix rows amongst banks to attain both command broadcasts and load-balance compute in banks (Section IV-A1 [a1](#), [a2](#)). To do so, for a given tile-size and input data-format (*line-18*), we sweep the tile-height ( $m\_tile$ ) from maximum possible (column-vector) to minimum (row-vector, *line-21*). Note that, we sweep tile-shape from column-vector towards row-vector, as this allows us to start with no cross-SIMD-lane operations and helps avoid their concomitant overheads. That said, our proposed sweep order does start with highest register pressure and we harness the sweep to meet register constraints (*line-26*). Our algorithm terminates when we identify a tile-shape that attains even distribution of matrix rows or we pick row-vector tile-shape.

2) *Tile-order Algorithm:* Algorithm 2 depicts our tile-order picking methodology. Recall that, tile-ordering aids in ensuring both that a matrix row is mapped to single bank in entirety (Section IV-A1 [a3](#)) and that DRAM row-locality is harnessed (Section IV-A1 [b2](#)). To realize both, we pick tiles first in column-major order (*line-12*), picking enough tiles to spread over available banks, before picking a tile in row-major order (*line-11*). This ensures that tiles within a matrix row (block) are mapped to same bank and same DRAM row (as possible by underlying row-buffer size and tile-size). As depicted in Figure 6, we term this order *column-row-order* or *CR-order*. As such, Algorithm 2 assumes that the tiled weight matrix is ordered in row-order fashion and outputs the tiles ordered in appropriate CR-order given the number of banks in the system.

### V. SOFTWARE CONSIDERATIONS AND ORCHESTRATION

#### A. Software and System Considerations

We discussed in Section IV how we balance myriad factors with our proposal PIMnast and derive optimized data-placement for GEMV-PIM. We discuss here how we realize

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**Algorithm 2** Find column-row-order (CR-order) of tiles
 

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1: function GETTILECROORDER
2:   Input: one-dimension array of PIM tiles tiled_matrix[], con-
   taining matrix [M, K] tiled with PIM tile [m_tile, k_tile] in row
   order, M, K, m_tile, k_tile, tot_bank
3:   Output: one-dimension array of PIM tiles tiled_cro_matrix[],
   containing matrix [M, K] tiled with PIM tile [m_tile, k_tile] in
   column-row-order
4:   m_TM = M/m_tile
5:   k_TM = K/k_tile
6:   tot_tile = m_TM × k_TM
7:   // num_abs - number of p contiguous all-bank spreads of
   tiles following M dimension. p is 1 here.
8:   num_abs = m_TM/(tot_bank × p)
9:   tile_per_abs = tot_bank × p × k_TM
10:  for q=0 to num_abs-1 do
11:    for cj=0 to k_TM-1 do
12:      for ri=0 to (tot_bank × p)-1 do
13:        tiled_cro_matrix[(q × tile_per_abs) + (cj ×
   tot_bank × p) + ri] = tiled_matrix[(q × tile_per_abs) +
   (ri × k_TM) + cj]
14:        ri ++
15:        cj ++
16:        q ++
17:  return tiled_cro_matrix[]
  
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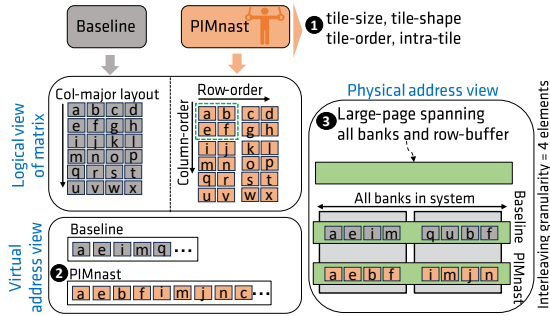


Fig. 7: PIMnast software and system considerations.

the resultant PIMnast data-placement in presence of system and software considerations.

1) *Realizing PIMnast Data-placement:* We depict the overview of changes necessary in Figure 7. First ❶, user employs PIMnast (Section IV-B) to deduce tile-size, tile-shape, tile-order and intra-tile-order (e.g., column major layout within a tile to avoid cross-SIMD-lane ops, Section IV-A). Recall that, PIMnast simply sets tile-size to interleaving granularity of underlying memory system without affecting it. Realizing other PIMnast recommendations requires that we first translate the resultant logical view of matrix (specific tile-shape and tile-order) to matrix’s virtual view via rearranging matrix elements in virtual address space ❷.

Next, we need to ensure that this virtual view is indeed realized in physical address space. Application address space is divided into virtual pages each of which maps to a system physical page (typically, 4KB, 64KB, 2MB, etc.). It is the system physical page which gets interleaved across banks/channel. A naive solution to translate PIMnast data-

placement would require physical page size as large as matrix size. However, we observe that, minimally, the page-size necessary is simply a product of interleaving-granularity and total number of banks across all channels as this allows the same command to be broadcasted to all banks (e.g., same vector element interacting with specific weight elements in banks). That said, to ensure DRAM row-locality is harnessed (Section IV-A), we ensure that the page-size also covers the row-buffers in banks (*preferred page-size*, depicted in Table I) as depicted in Figure 7 ❸. To cover potential memory configurations and future proof our proposal, we propose to employ a 2MB page size.

TABLE I: Page sizes necessary for PIMnast with interleaving granularity of 256bytes.

#channels	#banks	row-buffer size (KB)	preferred page-size (KB)
8	16	2	256
16	16	2	512

Note that, large pages can have associated challenges such as memory fragmentation. However, they also can have concomitant benefits such as lower TLB pressure and can be particularly beneficial for memory capacity heavy workloads like GenAI models. Note that, while optimized PIM data-placement requires large pages, there is no memory pinning requirement necessary for PIM acceleration. Finally, low-end systems with lower channel/bank counts can also potentially lower large page-size needed.

2) *Application Considerations for PIMnast Data-placement:* For GenAI inference scenario that we focus on, model weights are read-only and as such, proposed PIMnast data-placement can be a one-time cost to rearrange weight elements in virtual memory at model deployment. Note that, we only offload token-generation phase GEMVs to PIM which are memory-bandwidth bound (Section II-A). As such, weight matrices are read by the SoC (e.g., CPU, GPU) during prompt-phase. As PIMnast preserves the channel/bank parallelism by preserving interleaving granularity as observed in baseline and further as prompt-phase is largely compute-bound, proposed PIMnast data-placement does not affect prompt-phase performance. Finally, token-generation is the dominant phase for GenAI inference especially at low batch-sizes (Section VI-E) and our proposed data-placement considerably accelerates this phase.

### B. Orchestration Knobs

As discussed in Section III-B, in PIM, computation orchestration follows from data-placement chosen and is constrained by the command broadcast requirement in PIM. That said, we identify two specific knobs: register allocation and exploiting input vector reuse, that open up opportunities to tune computation orchestration in PIM for performance.

1) *Register Allocation:* Registers associated with PIM ALUs are the only low-overhead access scratchpad space available to PIM computations. Unlike CPUs/GPUs, only a handful of PIM registers are typically provisioned for area/cost

reasons. For GEMV-PIM, these registers primarily hold input-vector (IV) elements sent by the SoC and partial output vector (OV) elements before they are spilled to memory.

Appropriate allocation of registers can have an impact on performance. Specifically we observe that, as read-to-write (and write-to-read) DRAM turnaround overheads are incurred every time we switch between sending IV elements (writes) and MAC operations (reads), depicted in Figure 3b as ② and ③, lowering these overheads by sending IV elements in bulk by allocating registers for IV can be beneficial. Empirically, we observe that about eight registers help us amortize DRAM turnaround overheads and we follow this allocation (we discuss effect of alternate allocations in Section VI-C1).

2) *Optimizing Input-vector Reuse*: We further also observe that sending IV from SoC to PIM ALUs can comprise a non-significant fraction of execution time. If, post data-placement, each bank houses multiple row-blocks of W, IV sent from SoC can be reused across row-blocks by interleaving computation of two or more row-blocks and thus help lower the overhead of transmitting input vector. Note that, to allow such row-block interleaved computation, PIMnast data-placement simply has to change the tile-order picked to ensure multiple W row-blocks are placed in same DRAM row in a bank. In effect, this amounts to increasing the CR-degree we employ: while Algorithm 2 depicts CR-degree of 1, Algorithm 3 depicts how we pick an appropriate/larger CR-degree. Finally, note that, as CR-degree increases, OV register pressure increases as multiple partial outputs (per row-block) need to be remembered. As such, Algorithm 3 maximizes CR-degree subject to register constraints.

---

**Algorithm 3** Find maximum CR-order degree

---

```

1: function GETCROMAXDEGREE
2:   Input: M, m_tile, tot_bank, in_reg, out_reg, tot_reg
3:   Output: max_deg
4:   rowblk_per_bank = M/(m_tile × tot_bank)
5:   max_deg = cur_deg = 1
6:   while cur_deg ≤ rowblk_per_bank do
7:     if (cur_deg × out_reg) + in_reg ≤ tot_reg then
8:       // Found possible max degree
9:       max_deg = cur_deg
10:    cur_deg = cur_deg + 1
11:  return max_deg

```

---

## VI. EVALUATION

### A. Methodology

1) *System Overview*: In this work, we focus on GenAI inference deployments on client platforms (e.g., laptops). A modern laptop SoC comprises CPU cores, integrated graphics (GPU), and an AI Engine (AIE) specialized for AI computations, all of which are coupled with LPDDR memory. We assume, as an example, AMD Ryzen™ PRO 7040 Series processors comprising eight CPU cores, 12 compute units (of GPU cores), 16 AIE tiles, and eight channels of LPDDR5x-7500 memory for a peak memory bandwidth of 120 GB/s [9].

For our PIMnast evaluation, we assume the LPDDR memory is PIM enabled, with each LPDDR channel comprised of sixteen banks. With sixteen banks and with half the command rate as is possible for PIM commands, this translates to a best case PIM acceleration of 8×. However, with the penalty incurred for DRAM row-opens, the roofline PIM acceleration drops to about 7×. Further, in-line with PIM prototype [4], we assume sixteen registers per PIM ALU.

While we assume the above system setup, note first that, PIM bandwidth boost is dependent on memory banks and PIM command rate and is independent of SoC compute/other capabilities (Section II-B). Second, in the memory bandwidth-bound scenarios we focus on, PIM acceleration is upper-bounded largely by this memory bandwidth boost. As such, our subsequent analysis is more a function of baseline memory bandwidth and PIM bandwidth boost and is not tied to any particular client SoC system.

2) *GenAI Workloads*: We study a spectrum of model sizes up to 30B parameters similar to models from open pretrained transformers (OPT) suite [10]. We exclude the extremely large models (66B, 175B) as these are impractical on client platforms even with extreme low-precision for model weights. That said, as our data below depicts, PIM acceleration is stable for large models.

3) *Performance Models*: We analyze performance using analytical models as PIM is currently only available as part of functional prototypes [4], [6]. Further, SoC simulators are too cumbersome/impractical as we analyze end-to-end GenAI effects of PIM as well.

**GEMV-SoC Performance Model**. As discussed above, client SoCs are rich with diverse compute components (CPU, GPU, and AIE), each with its own compute throughput and available memory bandwidth. For GEMVs mapped to SoC, we optimistically assume the maximum compute throughput across all IP blocks (33.2 TOPS for 8b inputs) and full memory bandwidth available (120 GB/sec). Execution time for GEMV is the maximum of compute-time (GEMV ops/peaks TOPs) and memory-time (matrix bytes/memory bandwidth).

**GEMV-PIM Performance Model**. For GEMV mapped to PIM, we use an in-house DRAM-timing based performance model which assumes a PIM architecture representative of recent commercial PIM designs [4]–[6]. The PIM commands are issued by the SoC as special load/store accesses which bypass the caches and issued in-order by the memory controller to multiple banks in parallel [4]. Based on GEMV under consideration, data mapping (Section IV) and orchestration (Section V), we deduce the exact DRAM commands needed to orchestrate the computation and incorporate necessary overheads (e.g., DRAM row open overheads, read-to-write turnaround, etc.).

**GenAI End-to-end Performance Model**. To analyze GenAI inference end-to-end performance, we use an in-house roofline-based performance model which takes in as inputs a model hyperparameters (e.g., number of layers, layer size, etc.), SoC peak compute and memory bandwidth and determines the critical path (compute or memory) per operator in

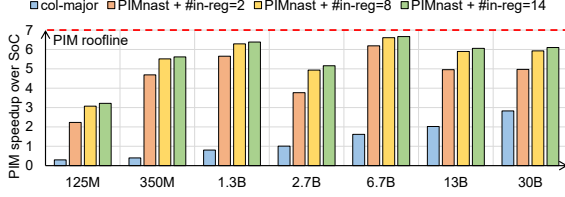


Fig. 8: PIMnast speedups with different register allocations.

the model to determine end-to-end metrics of interest such as per-token latency.

### B. Baseline PIMnast Speedups

In Figure 8, we first evaluate GEMV speedup for baseline PIMnast ( $PIMnast + \#in-reg=8$ , where  $\#in-reg$  is the number of registers holding input-vector elements sent by the SoC) and compare it to both roofline PIM acceleration possible ( $7\times$ ) and col-major data-placement<sup>3</sup>. The figure depicts average speedups across all GEMVs in token-generation (except attention GEMVs<sup>4</sup>), in all, four GEMVs per model. We assume 8bit data-format for weights/input-vector with 16bit accumulation.

As depicted in the figure, baseline PIMnast is able to boost GEMV performance by up to  $6.6\times$  across evaluated GenAI models compared to PIM roofline speedup ( $7\times$ ). As the figure depicts, col-major layout can even lead to slowdowns demonstrating the criticality of optimized data-placement for PIM. Overall, in comparison to col-major placement, PIMnast achieves up to  $25.7\times$  speedup (average  $5.4\times$ ).

While baseline PIMnast attains good speedups for most models, we also observe lower speedups for 125M and 2.7B models. This is so, as optimizing for load-balancing across banks causes short and wide tile-shapes which incur high overheads (e.g., sending of input-vector from SoC, etc.). We discuss techniques to address this in Section VI-F.

### C. Orchestration Knobs Speedups

We next discuss the effects of orchestration knobs (Section V-B) on PIM acceleration.

1) *Register Allocation Impact*: First, we vary registers allocated to input vector (IV) and depict two extreme configurations in Figure 8 in addition to PIMnast baseline. While baseline PIMnast allocates eight registers (half of available registers) to IV, we study scenarios where we allocate only two registers ( $PIMnast + \#in-reg=2$ ) and fourteen registers ( $PIMnast + \#in-reg=14$ ) respectively to IV. Allocating multiple registers to IV allows sending IV in chunks and lowers DRAM turnaround overheads leading to better performance as depicted. That said, going from fourteen to eight registers

<sup>3</sup>Note that, in presence of data interleaving as is present on most systems to harness memory parallelism, row-major data-placement leads to considerable overheads (e.g., inter-bank communication) and hence is not practical for PIM.

<sup>4</sup>Attention computation is a small fraction of execution time at batch-size 1 and involves dynamic data-placement in context of PIM and hence we map it to SoC.

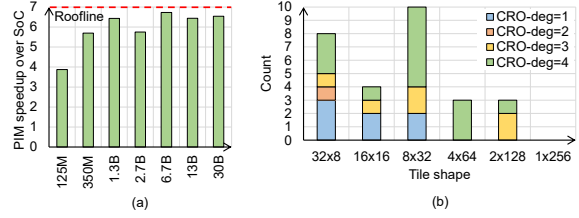


Fig. 9: PIMnast-opt (a) speedup and (b) selection breakdown.

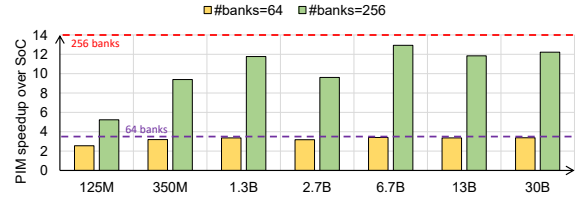


Fig. 10: PIMnast-opt speedup with varying  $\#banks$ .

only leads to a 3% drop in speedup and as such we allocate eight registers to input vector.

2) *Impact of CR-order degree*: Leaving eight registers free (of available sixteen) opens up opportunity to harness higher CR-order degree allowing reuse of IV across row-blocks of the input matrix. Recall that, higher CR-order degree interleaves computation of row-blocks and increases output vector (OV) register pressure as OV registers are per row-block. We depict the effect of maximizing CR-order in Figure 9(a) and term resultant design as **PIMnast-opt**. As depicted, maximizing CR-order degree allows PIMnast-opt to achieve speedup of up to  $6.86\times$  ( $5.8\times$  on average), attaining up to 35% higher speedups (10% on average) as compared to baseline PIMnast. This particularly helps models such as 125M (speedup of  $3.88\times$  versus  $3.07\times$ ). We assume PIMnast-opt for all subsequent results.

Finally, we also depict in Figure 9(b) the breakdown of the tile-shapes and CR-order degree picked across all GEMVs we model. As depicted, our proposed PIMnast methodology picks a variety of tile-shapes and CR-order degrees to maximize PIM acceleration.

### D. PIMnast Resiliency

Next, we evaluate the resiliency of proposed PIMnast methodology across spectrum of memory configurations, GenAI needs, and PIM architecture sweeps.

1) *Memory Configuration Sweep*: We study two parameters for memory configuration.

**Number of Banks**: We first evaluate the robustness of PIMnast methodology by hypothetically varying the number of banks per channel. Figure 10 depicts results for  $2\times$  lower (64 banks in the system) and higher  $\#banks$  (256 banks in the system) than baseline setup we have. As banks are the compute workhorses in PIM, varying the  $\#banks$  in the system also changes the PIM roofline speedup to about  $3.5\times$  and  $14\times$



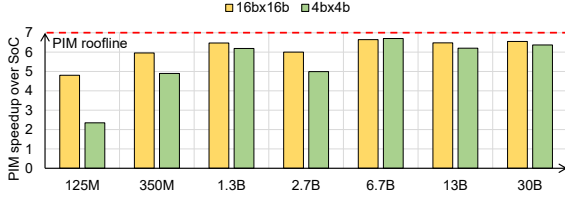


Fig. 11: PIMnast-opt speedup with varying data-formats.

respectively. With  $2\times$  lower banks, PIMnast-opt attains up to  $3.43\times$  (average  $3.2\times$ ) of available  $3.5\times$  roofline speedup, while with  $2\times$  higher banks, PIMnast-opt attains up to  $13.5\times$  (average  $10.1\times$ ) of available  $14\times$  roofline speedup demonstrating the resiliency of PIMnast methodology to varying #banks.

**Interleaving Granularity:** Recall that PIMnast sets tile-size to interleaving granularity of underlying memory system. Changing interleaving granularity does not affect PIMnast-opt speedup as a key tenet of our data-placement is we aim to balance matrix rows between banks (Section IV-B,  $m_{\text{tile}}$  of resultant tiles) and as such, different interleaving granularities can be subsumed by adjusting  $k_{\text{tile}}$  while preserving  $m_{\text{tile}}$ .

2) *GenAI Needs Sweep:* We study two GenAI needs namely, data-formats and scale-factors.

**Data-formats:** Our results here forth assume 8bit data-format for weights/input-vector. Next, we vary data-formats and depict resultant PIM acceleration in Figure 11. As shown in the figure, our proposed flexible data-placement and orchestration methodology unlocks an average PIM speedup of  $5.1\times$  and  $6.1\times$  for 4b and 16b data-formats, respectively. While the acceleration is similar across data-formats, for some models, PIM acceleration drops for 4b. This is because the effects of wider tile-shapes in models such as 125M are further exacerbated as precision drops.

**Scale-factors:** In Figure 12, we show the performance of PIMnast-opt in presence of block-level scale-factors (block-size of 32 [11]). Recall that, low-precision inference (8b, 4b and lower) often relies on block-level scale-factors [8]. In the context of GEMV, with block-level scale-factors, computation of single output element is interspersed with multiplication of partial outputs with both weight and input-vector scale-factors. With added overhead of these multiplications, PIM acceleration drops in presence of scale-factors. Regardless, PIMnast-opt attains up to  $6.1\times$  (average  $4.1\times$ ) for 8b formats and up to  $6.4\times$  (average  $3.1\times$ ) for 4b, respectively.

We also studied the effect of larger block-sizes (not shown) on PIMnast-opt acceleration and observed increased PIM speedup for both 8b and 4b because the overhead of processing scale-factors reduces as block-size increases. For example, under 8b inputs, a block-size of 64 and 128 elements results in a speedup boost of up to 34% and 61% (14% and 23%, on average) compared to block-size of 32.

3) *PIM Architecture Sweep:* With regards to PIM architecture, we vary available registers within PIM ALU and study

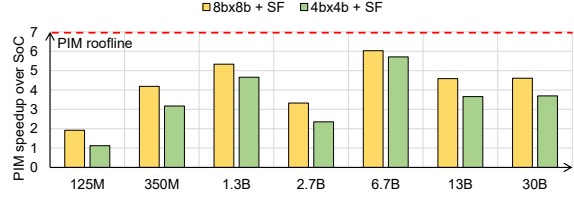


Fig. 12: PIMnast-opt speedup with block-level scale-factors.

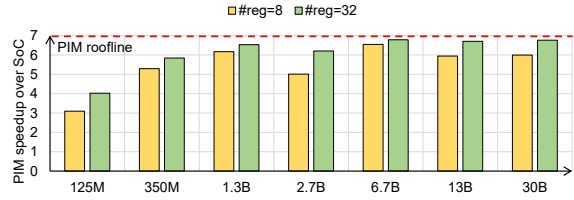


Fig. 13: PIMnast-opt speedup with varying #PIM registers.

half as many and twice as many PIM registers as baseline configuration. We follow the same register allocation strategy in the sweep (equal registers to IV and OV). We depict the resultant PIM acceleration in Figure 13. As depicted in the figure, PIMnast-opt adapts its data-placement and orchestration to the available register count. Specifically, with half as many registers, PIMnast-opt maintains a maximum PIM speedup of up to  $6.6\times$  ( $5.3\times$  on average). Similarly, with twice as many registers, we observe up to  $6.9\times$  speedup ( $6\times$  on average). Note that, with more registers, there are ample opportunities for different register allocation mechanisms unlocking further acceleration and we leave exploring these to future work.

#### E. PIMnast GenAI End-to-end Speedups

We depict in Figure 14 both per-token latency speedups and end-to-end speedups (prompt + token-generation) with PIMnast-opt assuming a prompt-size of 1920 and 128 generated tokens. As tokens are generated one at a time, token-generation dominates GenAI inference time, especially in the case of low batch-sizes [12]. Similarly, using our GenAI end-to-end performance model, we observe that about 88% or more of time is spent in token-generation (not shown). Therefore, across a spectrum of GenAI models, PIMnast-opt delivers up to  $5\times$  ( $3.5\times$  on average) speedups for per-token latencies translating to end-to-end speedups of up to  $3.5\times$  ( $2.7\times$  on average). The speedups PIM realizes can open-up exciting possibilities with regards to client platforms. To name a few, it can enable larger/more accurate models to be deployed at low latencies, make possible chains of models one feeding the other, and more.

#### F. Addressing PIMnast Deficiencies

In this section, we evaluate potential optimizations (both hardware and software) to address the low PIMnast-opt

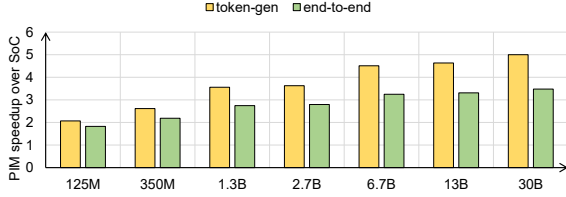


Fig. 14: GenAI end-to-end speedups with PIMnast-opt.

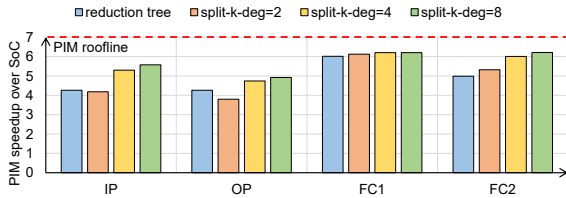


Fig. 15: PIMnast-opt speedups with h/w and s/w optimizations for 125M model.

speedup for certain GenAI models (e.g., 125M). We identify two optimizations that make a difference.

**Hardware - Support for cross-SIMD operations:** As discussed above, a key factor for the low performance with PIMnast-opt is when tile-shapes are very short and wide incurring cross-SIMD lane computations. As such, PIM ALU with efficient cross-SIMD lane support such as a reduction tree [13] can address this cost. As we depict in Figure 15, such support can attain an upper-bound speedup boost of up to 41% (25% on average) compared to PIMnast-opt for 125M model.

**Software - Split-K:** In scenarios where weight matrix has small  $M$  dimension, to avoid the scenario where we end up with fewer row-blocks to distribute across banks, PIMnast picks short, wide tile-shape which leads to lower IV reuse and triggers cross-SIMD lane compute. An alternate mechanism can vertically decompose the matrix  $M \times K$  into  $2^i$  parts, each of size  $M \times (K/2^i)$  where  $i \geq 1$ , each processed by a subset of the channels. This effectively avails more row-blocks and therefore allows picking a taller tile-shape. A downside however is each bank only has partial result requiring SoC to perform final reduction incurring software complexity. We refer to this software optimization as *split-K*. Figure 15 depicts the resultant PIMnast-opt acceleration in presence of varying split-K degrees (*split-k-deg*) up to eight splits for the four GEMVs manifested in 125M model. We observe that as split-K degree increases, PIMnast-opt boosts speedup by up to 85% (47% on average) compared to not using the split-K optimization.

## VII. DISCUSSION

This work focuses on optimizing data-placement to accelerate GEMVs with PIM. That said, this paper does identify a comprehensive list of PIM architecture and memory related

factors that affect data-placement, and proposes *broad* strategies to tackle these inherent factors. The key strategies are:

- Identify and distribute compute-independent data amongst banks (Section IV-A1 e.g., matrix rows in GEMV computation).
- Within a compute-independent data block, data-placement is adjusted (Section IV-A1 e.g., column major data-placement within a DRAM row).
- Tile the compute-independent data blocks and swizzle the tiles in the virtual memory (Section IV-A2).
- Adjust the tile’s shape to manage the register constraints (Section IV-B1).
- Harness large pages to realize the required data-placement (Section V-A1).

Above methodology extends beyond GEMVs and can be applied to accelerate other primitives and workloads of import such as fast Fourier transforms (FFTs) and sorting. For example, above methodology extends to accelerating FFT with PIM as follows (also shown in Pimacolaba [14] as well):

- A batch of independent 1D FFTs (or within 2D FFT) is identified as the compute-independent data block to distribute amongst the banks.
- Within the batches of 1D FFTs, the FFT elements are strided to avoid cross-SIMD-lane communication.
- The batches of 1D FFTs are tiled and swizzled in the virtual memory and large pages are harnessed.

## VIII. RELATED WORK

GEMM/V are critical primitives in many key workloads such as GenAI. Therefore, there exist many vendor provided GEMM/V libraries for CPUs [15], [16] and GPUs [17]–[20] as well as hardware innovations such as GPU matrix cores [21], [22] that are employed to accelerate such primitives. In addition to general-purpose CPUs and GPUs, many recent accelerators arise to boost GenAI performance [23], [24]. However, such hardware solutions are targeted towards cloud-based GenAI. In this work, we focus on accelerating the GEMVs that manifest in GenAI on client platforms with PIM-enabled LPDDR.

There exist many prior work that boost GEMM/V performance using possible commercial PIM designs. Oliveira *et al.* provide a high-level analysis of GEMV acceleration using UPMEM, a server-based PIM system [25]. However, the authors do not discuss their data-placement or any optimizations employed. Sura *et al.* propose computing system called Active Memory Cube (AMC) with in-memory processors to accelerate GEMMs and other workloads [26]. AMC employs large register files of 16KB per in-memory ALU to improve data reuse. Newton [13] presents GEMV data placement for a possible commercial PIM architecture, which is similar to what we assume. Newton assumes very large memory interleaving granularity matching DRAM row size, which becomes unrealistic when host and PIM use same memory space. Moreover, it chooses to use fixed tile shape for any matrices and do not consider possible benefit of bank locality

of matrix data mapping, and hence heavily involves host to perform the reduction of partial sums to get the final output, unlike PIMnast. StepStone PIM [27] targets optimizing similar ML domain as us; however, the underlying PIM architecture considered is much different. It targets to solve impact of address hashing in localizing GEMM operands per PIM unit by employing an address generation logic which facilitates temporal locality of input matrix elements in PIM execution, though it still needs input vector(s) replication per PIM unit and output reduction. Also, variable matrix sizes and shapes impact performance of StepStone when PIM units are closely placed to memory banks. In PIMnast we provide mapping solution for such variability. Compared to PIM designs incurring considerable area overheads due to significant changes to DRAM, or having PIM and non-PIM memory spaces (which requires memory copies) [26], [28], or using speculative technology (e.g., memristor [29]), PIMnast focuses on commercially viable PIM designs getting wide traction as evident by multiple memory vendors converging to this design [4]–[6].

Finally, many works exploit PIM’s data movement reduction and performance boost to accelerate key ML and HPC workloads [4], [14], [30]–[35]. To the best of our knowledge, this is the first work to investigate the myriad factors affecting data-placement on PIM to come up with methodologies to effectively map GEMV computations to commercially-viable PIM designs, hence harnessing PIM bandwidth boost.

## IX. CONCLUSION

This work focuses on maximizing acceleration for matrix-vector multiplications (GEMVs) using commercial processing-in-memory (PIM) prototypes made available by memory vendors. We observe here that deducing optimized data-placements is critical to harness PIM acceleration. To this end, we identify factors affecting data-placements, propose matrix tiling/ordering algorithms to tackle these factors and identify orchestration knobs that impact PIM acceleration. Overall, our proposed ideas deliver up to  $6.86\times$  speedup of the available  $7\times$  roofline speedup leading to up to  $5\times$  speedup for per-token latencies for a spectrum of GenAI models.

## ACKNOWLEDGMENT

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